Andrew Peck

Electronics Engineer

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Skills

- **Electronic System design:** experienced with bringing many large-scale hardware and FPGA firmware projects from conception to completion, including system design, budgeting, planning, electronics design, firmware and software, parts procurement, production, testing, and support; oversight and training of numerous students/junior engineers, collaboration with physicists & translation of vague requirements and algorithms into concrete systems designs.
- **FPGA firmware design and validation:** 13 years of experience in firmware development/testing of both low level features and high level algorithm / control system design and implementation. Strong knowledge of low-level features of Xilinx FPGAs, including multi-gigabit links, clock resources, SERDES interfaces, memory, AXI, Zynq integration, Vivado Tcl scripting. VHDL/SystemVerilog, CocoTb, Vivado, QuestaSim, Verilator, GHDL.
- **Digital and analog schematic and PCB design:** specialized in digital electronics but with some experience in analog aspects of electronics instrumentation (amplifiers, filters, analog front ends, etc). Altium, OrCAD/Allegro, KiCAD, LTSpice.
- **Software and scripting:** experienced in a variety of software projects, at all levels from drivers for embedded CPUs to high-level experimental control and analysis software, along with modeling/simulation of complex systems. Python, Lisp, Tcl, C, Git, Linux, LaTex, Gitlab CI, Docker, Awk.

Job History

Manager, Control System Architecture — Palo Alto, CA
PsiQuantum Inc — August 2023 – Present

Consultant — Los Angeles, CA
General Antiparticle Spectrometer — February 2018 – Present

Electronics Engineer — Boston, MA
Boston University Electronics Design Facility — February 2020 – August 2023

Electronics Engineer — Los Angeles, CA
UCLA Department of Physics — January 2013 – January 2020

Undergraduate Researcher — Los Angeles, CA
UCLA Astroparticle Physics — July 2012 – December 2012

Administrative Assistant — Pasadena, CA
Caltech/MIT Enterprise Forum — January 2009 – July 2010

Administrative Assistant — Pasadena, CA
Entretech — May 2007 – January 2009

Laboratory Assistant — Pasadena, CA
California Institute of Technology — June 2007 – September 2007

Education

Bachelor of Science, Physics — Graduated December 2012
University of California, Los Angeles

Selected Projects

Below I have selected some major projects that I have worked on; in each of these projects I was the primary or co-designer of the electronics and played a leading role in the development of the system. I am proud to share much of my work at github.com/andrewpeck. I also have a more comprehensive listing of my past work which is viewable at andrewpeck.xyz/projects.html

PsiQuantum Control System

- Worked with physicists to design, and led the hardware implementation of low latency, real-time control algorithms for photonic systems. Wrote implementations in Verilog targeting several Xilinx FPGAs with logic clocked at 500 MHz. Developed cycle-accurate python models to be integrated into quantum+classical system models. Simulation with CocoTB/Verilator, modeling in proprietary Python event-based simulation framework.
- Developed a library of re-useable Verilog components (sorters, binary tree comparator, adder trees, priority encoders, running sums, programmable delays, pseudo-random number generators, etc.)
- Trained and supervised a small team of digital design engineers.
- Set up Gitlab continuous integration for automated compilation/release of Xilinx FPGA projects.
- Set up Gitlab continuous integration for documentation deployment; created and maintained several Docker images for HDL simulation, documentation, Xilinx FPGA compilation, etc.
- Led initial design and debug of several core FPGA projects (e.g. detector digitizer, switch driver).
- Led the effort for system documentation and electronics/logic requirements definition and tracking. Played a central role in communication of system design, goals, and requirements to other teams.
- Assisted other engineers with digital design/debug, printed circuit development.
- Review of printed circuit boards, review of digital designs.
- Co-designed the electronics system architecture (PCB high level requirements, FPGA choices, data link speeds, connectivity, etc).

GAPS Time of Flight Electronics

- Co-designer of the readout and trigger electronics for the time of flight (TOF) system of the General Antiparticle Spectrometer (GAPS). Involved in the experiment since it was in the prototype stage, and played a major role in guiding the design of the readout and trigger system for the TOF.
- Codesigned the schematic/PCB for a 5 Gsps 8 channel waveform digitizer ASIC read out by a Zynq SOC.
- Wrote Zynq FPGA firmware which controls and reads out the Zynq waveform digitizer, deserializes trigger info, packetizing and buffering data,and transferring it into the Linux processing system through DMA.
- Co-designed the GAPS master trigger electronics schematic/PCB.
- Wrote all master trigger FPGA firmware, which deserializes data from 400 detector channels (received via 200 Mbps oversampled asynchronous LVDS links), performs low latency trigger logic to identify characteristic decay signatures, and serializes trigger information to the readout boards and the tracker DAQ. The firmware also has a GbE UDP interface for control and readout of the trigger information, and SPI/I2C interfaces for monitoring.

CMS Cathode Strip Chambers

- Designed two different FPGA based data concentrator cards hosting Spartan-6 LX75 and LX150T FPGAs with multi-gigabit optical readout. Handled all steps of the design, procurement, production, design of testing jigs, test procedures, and test software/firmware; oversaw a cohort of undergraduate students to perform QA testing on boards; diagnosis and repair of faulty electronics.
- Was responsible for the fabrication and testing of 3200 ASICs used for the readout of the detector: worked with IMEC to fabricate and dice the silicon and get the chips packaged; designed a test board featuring an Atmel 32-bit MCU with a Spartan-6 FPGA that drives a programmable analog pulse injection circuit

and reads out the digital response of the ASIC; wrote the MCU firmware, FPGA firmware, C++ readout software (through USB), a C++ data analysis suite that collected channel data and performed fitting / histogramming to determine pass/fail for each chip. A chip socket was used to hand test each of the ASICs, which are being used for data taking on the CMS detector.

CMS GEM Electronics

- Co-designed the readout electronics for the Gas Electron Multiplier (GEM) subsystem of the CMS detector at CERN; I had a broad role in the development of the project, taking part in conceptual design, schedule, costing, electronics design, and production of electronics for the readout of more than 1 million detector channels.
- Wrote the data concentration firmware for the GE11 and GE21 subsystems; I designed firmware targeting Artix-7 and Virtex-6 FPGAs which takes in 112 Gbps of data on 320 Mbps links and concentrates it onto an optical fiber at 4.0 Gbps using a custom-designed zero suppression scheme that performs lossy 14:1 data concentration with an algorithmic latency budget of only 100 ns.
- Designed the data concentrator card for the ME0 subsystem which is responsible for receiving data and serializing it onto 10 Gbps optical links. Was responsible for schematic capture, layout, prototype fabrication and testing, and development of testing scripts.
- Designed and implemented the ME0 segment finder, which is a custom firmware block that processes 368 Gbps of data and performs multi-layer pattern recognition and sorting to identify patterns of hits corresponding to charged particles passing through the detector. This design targeted a Xilinx VU13P FPGA and is now in the early stages of testing in hardware.

CMS MIP Timing Detector Readout

- Helped develop the electronics for a precision timing detector which consists of nearly 11 million detector channels each capable of time-tagged charged particles with a precision of ¡50 ps. I was responsible for a prototype of the readout board, which is a data concentrator card that serializes detector data onto 10 Gbps optical links.
- Designed a data acquisition system based on a Kintex Ultrascale FPGA that deserializes data from the readout board, decodes the ASIC data format, does consistency checking and buffering of data, and reads out data through a GbE link. Also co-designed the readout and control software.
- Co-designed a frontend mixed-signal 'module PCB', that hosts four front-end ASICs and sensors which are wire-bonded to the board.

ATLAS L0 Muon Drift Tube Trigger

- Wrote the hardware interfaces for the L0MDT trigger FPGA (frontend interface, backend interface, control plane interface).
- Worked with other engineers to integrate algorithmic payload firmware.
- Extensive review of printed circuit schematics and layouts for several PCBs.
- Assisted other engineers with optimizing implementation of algorithms.

CMS OCEAN

- I worked with a junior engineer to build several smaller prototypes along a complex electronics design which features a large Xilinx ZU19EG FPGA, high current power supplies, SATA, USB, DDR4, Gigabit Ethernet, display port, and 72 optical links operating at 25 Gbps, while confirming to the ATCA specification.