F14 "Tom Cat" Central Air Data Computer (CADC)

Ray & Bill Holt hired (June 1968)

Final requirements for the CADC from Grumman Aircraft released (August 1968)

Steve Geller & Ray Holt was given the task for the microprocessor
(other CADC tasks include sensors, mechanical to electronic convertors, power supply, math, packaging, testing, prototyping, drafting, administration)

Biil McCormick, Applied Mathematician worked on the aerospace math equations. Bill McCormick's actual math skribbles on the right.

this procedure.

MATHEMATICAL MODEL AND SCALING CONSIDERATIONS

The system problem statement is defined in terms of mathematical equatio[ns]. An example of this is as the following polynomial:

Input Y, Output E

$$E = \sum_{i=0}^{3} a_i X^i = X^3 a_3 + X^2 a_2 + X^1 a_1 + a_0 = \text{3rd order polynomial}$$

where,

$$X = \frac{Y\Big|_{L1}^{L2} + B}{C}$$

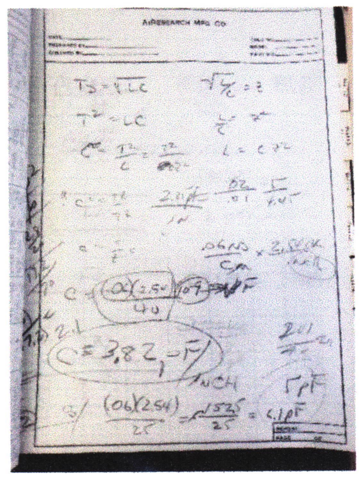
This represents a third order polynomial whose independent variable is conditioned (B), expanded (C), and limited (L1, L2). This example will be used throughout the entire software procedure.

The math model should be appropriately scaled such that no calculations will exceed $\pm (1-2^{-19})$. These are the maximum positive and negative values obtainable in the processor. A few rules that should be followed when doing the scaling are as follows:

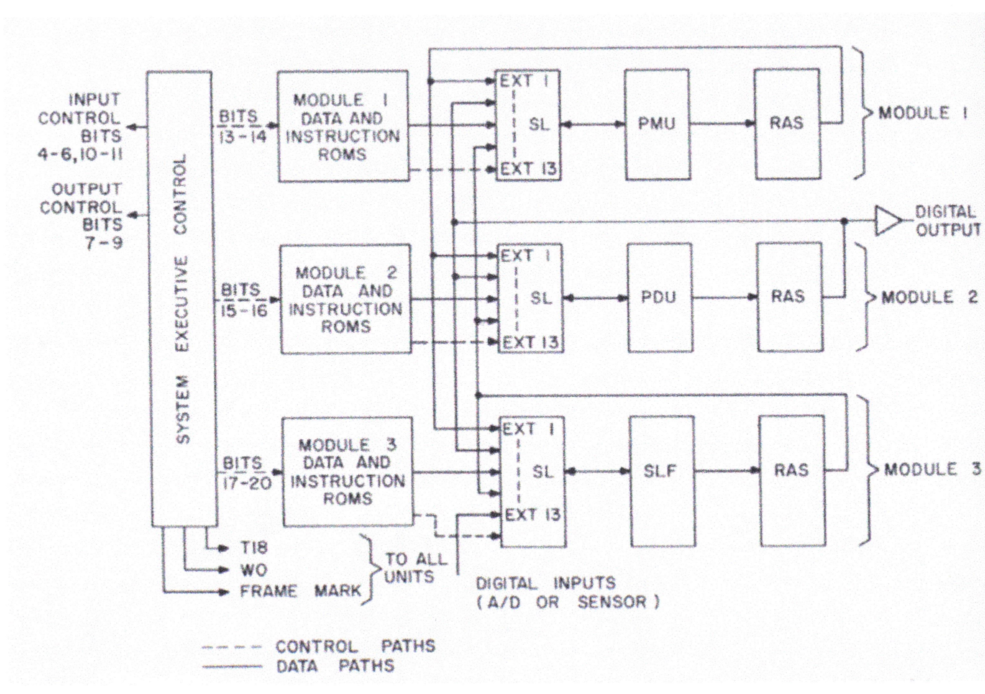
... be scaled to the ...

$$\alpha_T = \underbrace{f_1\left(\frac{Psi}{Pti}\right)}_{\text{SLOPE}} \alpha_i + \underbrace{f_2\left(\frac{Psi}{Pti}\right)}_{\text{INTERCEPT}}$$

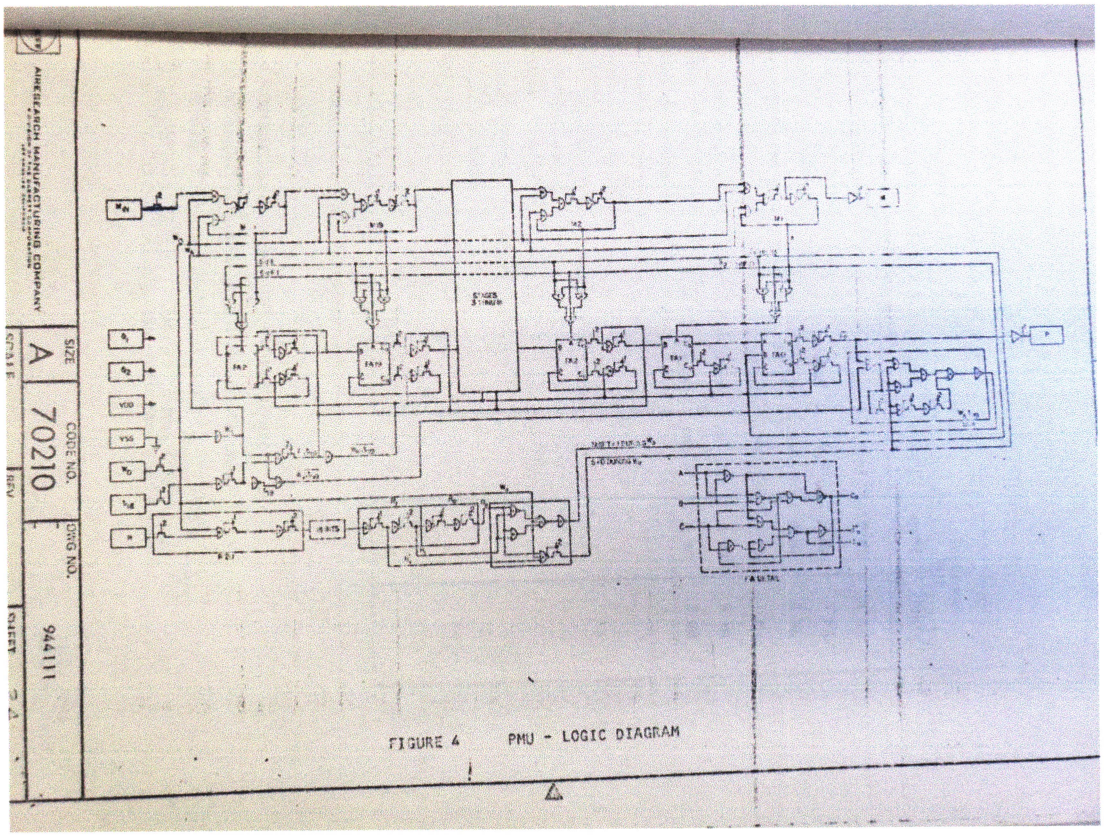
$$\frac{\alpha_T}{K_I} = \left[\frac{\left(\frac{\sum_{i=0}^{6} a_i X^i}{K_2}\right)}{K_3}\right]\left(\frac{\Sigma\alpha_i}{50}\right) + \left(\frac{\sum_{i=0}^{6} b_i Z^i}{K_I}\right)$$



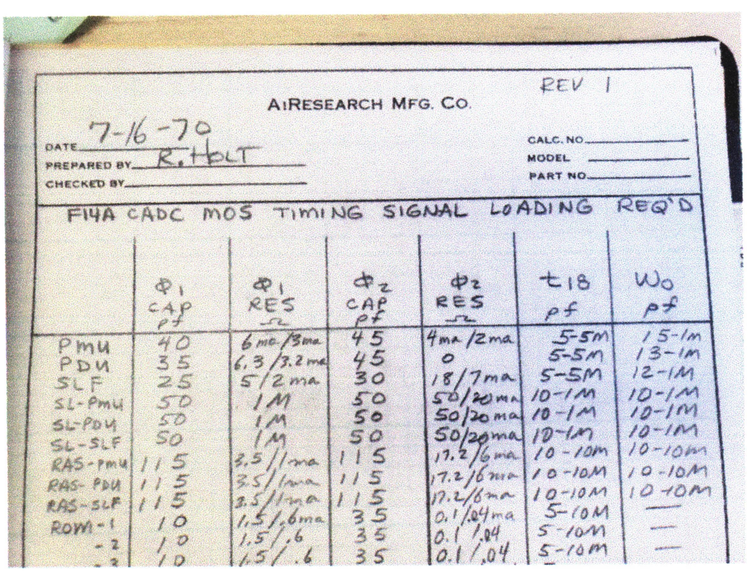
Steve Geller worked on the big picture concept called System Design. (August 1968 – March 1969)



Ray worked on detailed implementation of the microprocessor chips called Logic Design. American MicroSystems designed the layout of the chips. Here is a small sample of logic design from one chip.



Major considerations of the microprocessor were: Size of Chips, Speed of Chips, Operating temperature of the Chips. All three together determined if the chips could be manufactured or not. We had to analyze every chips electrical condition and the clock timing to make sure they would work at the military temperature range.



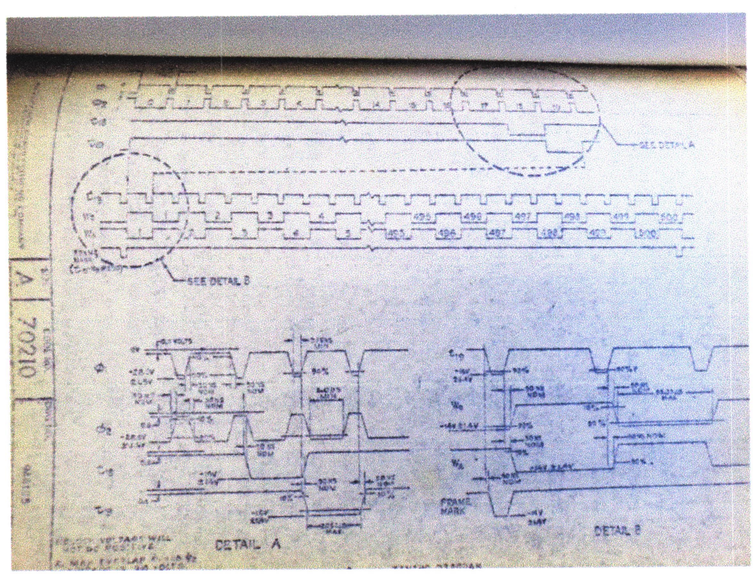
AIRESEARCH MFG. CO.

REV 1

DATE 7-16-70
PREPARED BY R. HOLT
CHECKED BY
CALC. NO.
MODEL
PART NO.

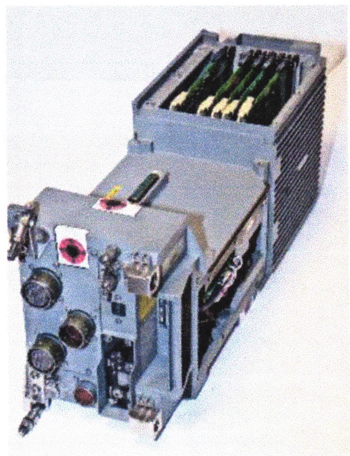
F14A CADC MOS TIMING SIGNAL LOADING REQ'D

	Φ1 CAP pf	Φ1 RES Ω	Φ2 CAP pf	Φ2 RES Ω	t18 pf	Wo pf
PMU	40	6ma/3ma	45	4ma/2ma	5-5M	15-1M
PDU	35	6.3/3.2ma	45	0	5-5M	13-1M
SLF	25	5/2ma	30	18/7ma	5-5M	12-1M
SL-PMU	50	1M	50	50/20ma	10-1M	10-1M
SL-PDU	50	1M	50	50/20ma	10-1M	10-1M
SL-SLF	50	1M	50	50/20ma	10-1M	10-1M
RAS-PMU	115	3.5/1ma	115	17.2/6ma	10-10M	10-10M
RAS-PDU	115	3.5/1ma	115	17.2/6ma	10-10M	10-10M
RAS-SLF	115	3.5/1ma	115	17.2/6ma	10-10M	10-10M
ROM-1	10	1.5/.6ma	35	0.1/.04ma	5-10M	—
-2	10	1.5/.6	35	0.1/.04	5-10M	—
-3	10	1.5/.6	35	0.1/.04	5-10M	—

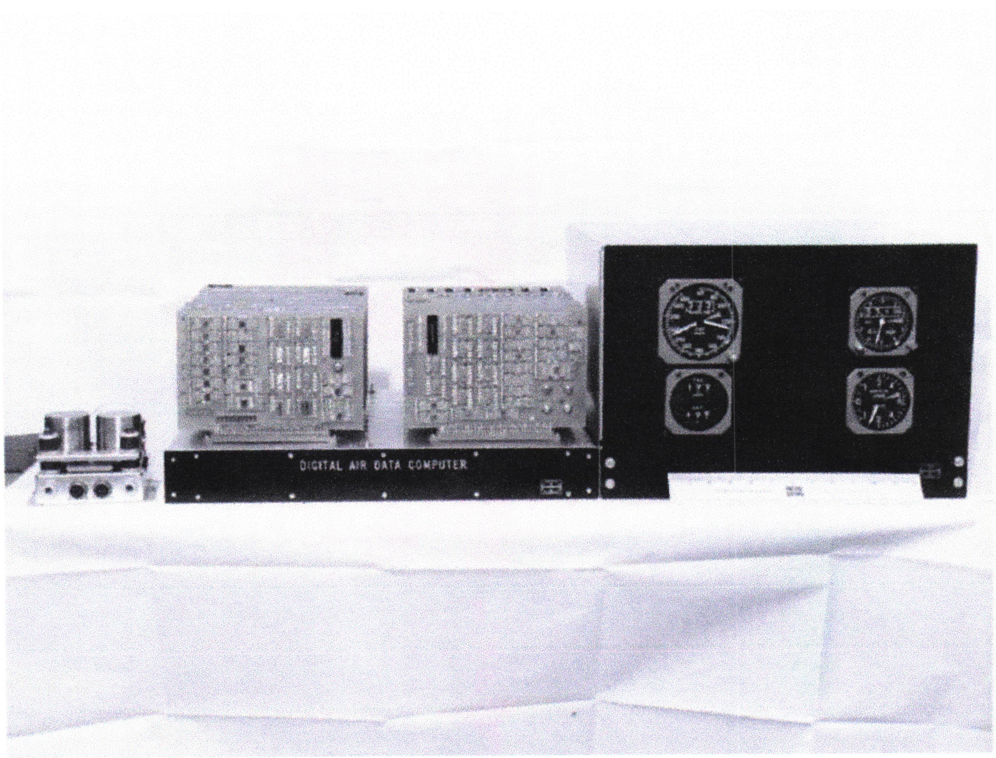


Over a six month period we worked with American MicroSystems (AMI) and had to rework from the System Design to the Logic Design THREE times. AMI would decide if they could make the chips and I would decide if the logic of the chips would work. The mathematics would rarely change.

Once we decided that we had a design that would produce working chips and AMI decided they could make them Garrett had to make the completed box and put the chips on circuit cards along with the sensor electronics and power supply.



While the Garrett engineers, such as Tom Redfern, were working on the box Ray Holt and Lynn Hawkins built a working prototype of the microprocessor out of standard available electronic circuits. This process took many months. This was the first proof that all the electronics would work together.



The next step was to exhaustively software simulate all the mathematics and logic design to make sure there were no hidden problems while we exercised the limits of the sensor inputs and outputs to the pilot gauges and for the wing sweep. The software simulator had the capability to find problems not revealed with the hardware simulator prototype. Bill Holt was the programmer on the software simulator. The software simulation produced expected values at every point inside the chips. This way we could determine if the design was working properly This process took several months.

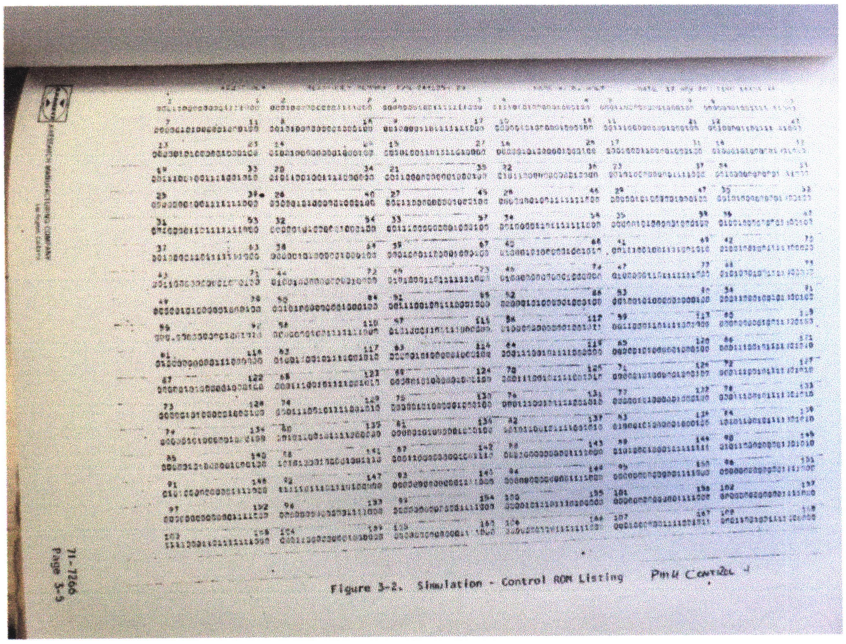

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Figure 3-2. Simulation - Control ROM Listing

Next, we had to start programming the chips to perform all the mathematics for the F14. The entire program ran in 1/16 sec and was repeated continuously. Every second the computer has to perform 5490 multiples, 1922 divides, 293 additions and subtractions, 73 square roots, and 842 inputs from sensors and outputs to gauges and the wing sweep. Once the program was proven to work, using the software simulation, the program code (binary 1's and 0's) had to be permanently manufactured into the Read-Only Memory program chips. This means if anything is incorrect the chip would have to be re-manufactured which, at that time, would take 2-3 months ... thus delaying the F14 flight tests.

Since we did not have time to develop and software tools (assemblers and compilers) to help the programming I had to program the microprocessor manually using binary 1's and 0's. Here are the steps I used to produce the program.

1. Convert all the math equations to a sequence of math defined blocks.

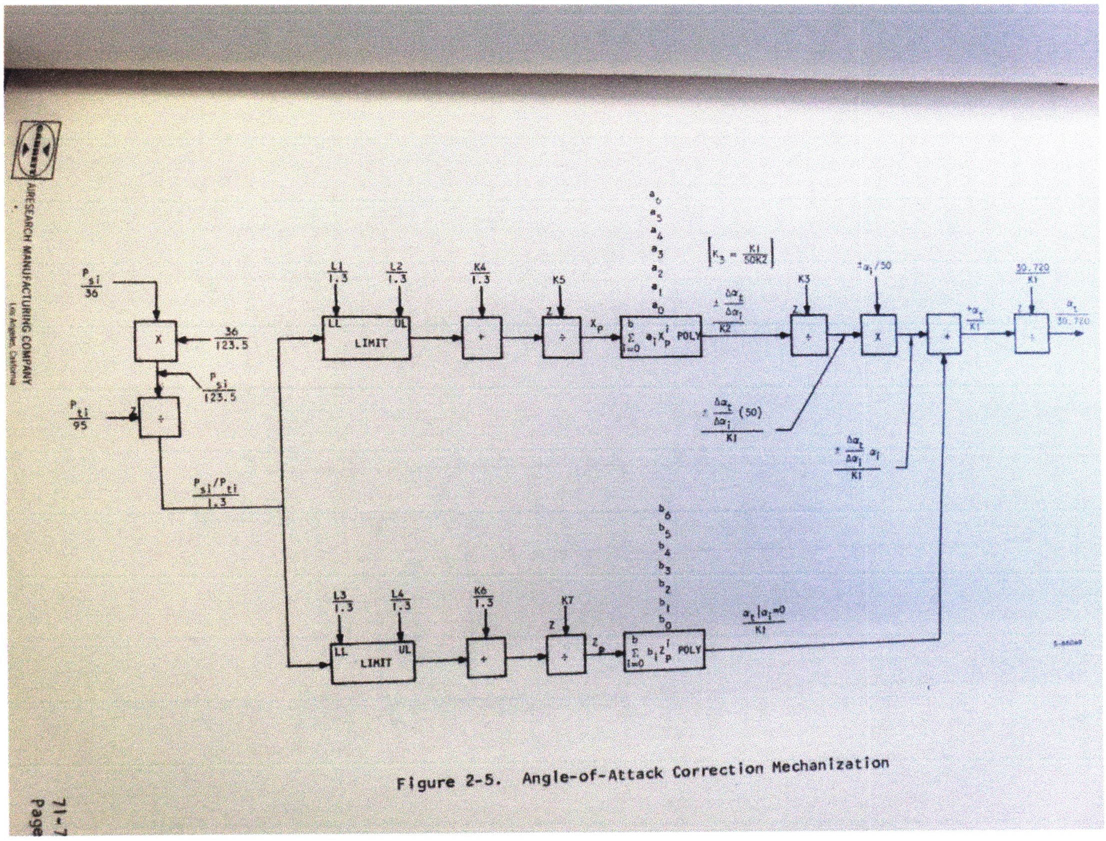


Figure 2-5. Angle-of-Attack Correction Mechanization

2. Convert the sequence of math blocks to the computers real-time sequence. This involved intertwining all the math equations based on real time.

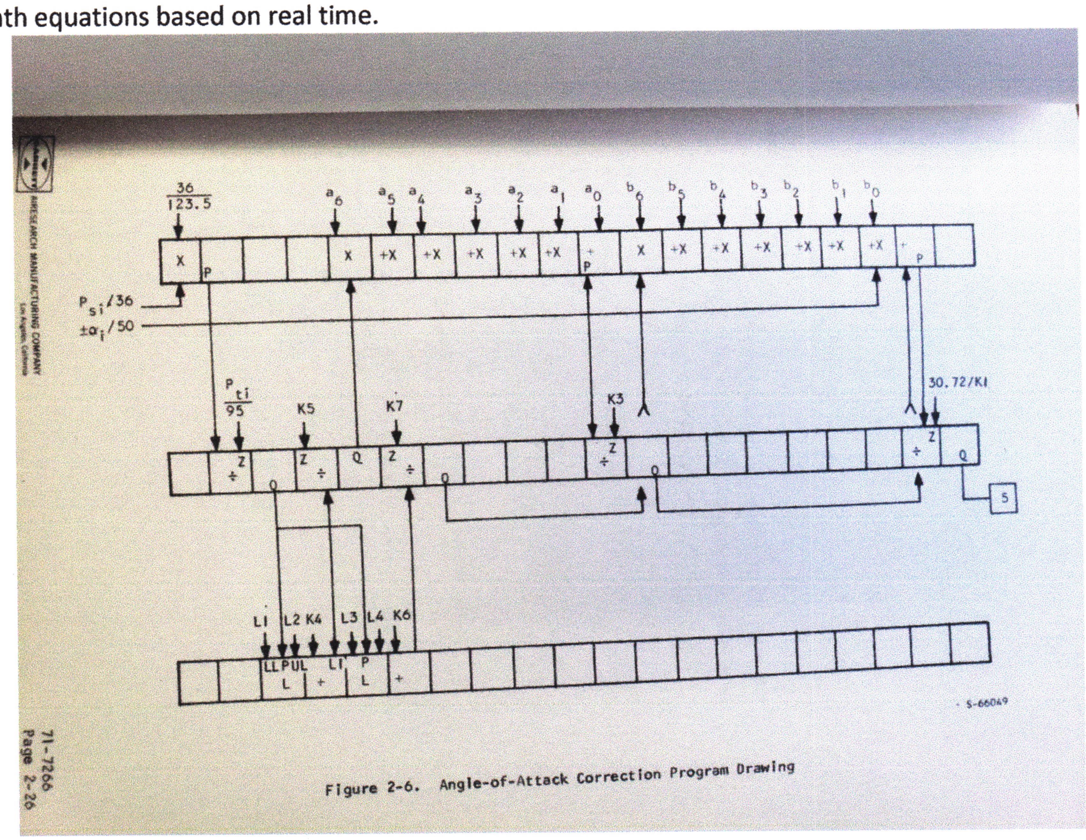
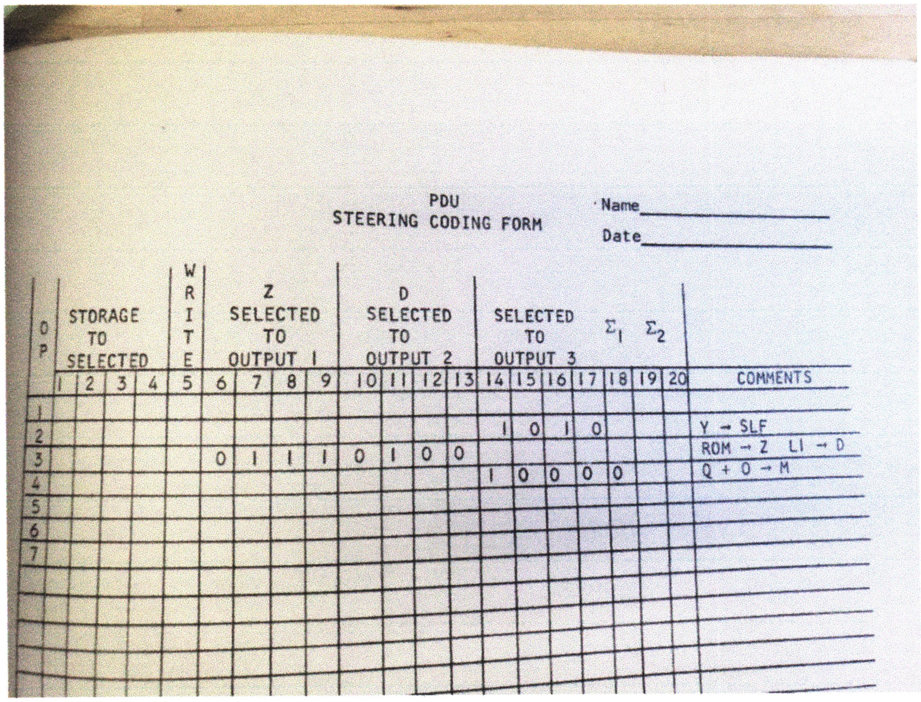


Figure 2-6. Angle-of-Attack Correction Program Drawing

3. Produce charts of 1's and 0's that would cause the microprocessor chips to perform the math equations. The entire program had 70,000 1's and 0's.



PDU
STEERING CODING FORM

Name____________

Date____________

OP	STORAGE TO SELECTED				WRITE	Z SELECTED TO OUTPUT 1				D SELECTED TO OUTPUT 2				SELECTED TO OUTPUT 3				Σ_1	Σ_2		
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	COMMENTS
1																					
2														1	0	1	0				Y → SLF
3						0	1	1	1	0	1	0	0								ROM → Z LI → D
4														1	0	0	0	0			Q + 0 → M
5																					
6																					
7																					

4. Test the final binary 1's and 0's code with the software and hardware simulator.

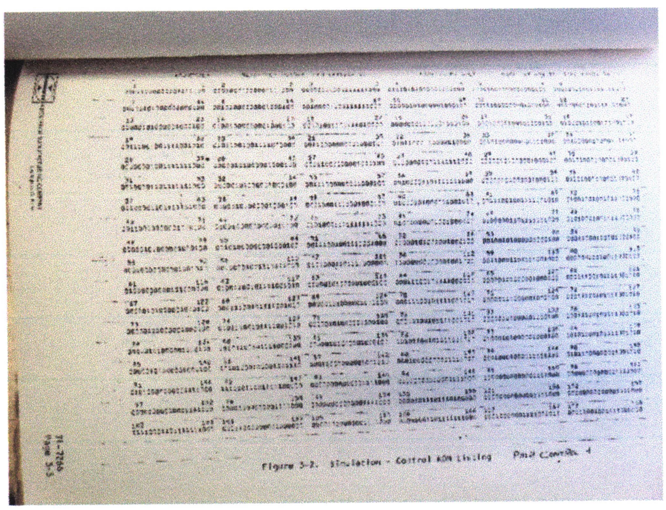
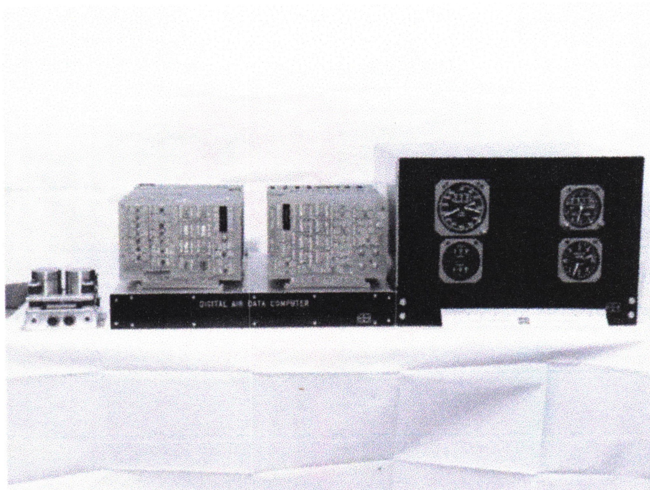
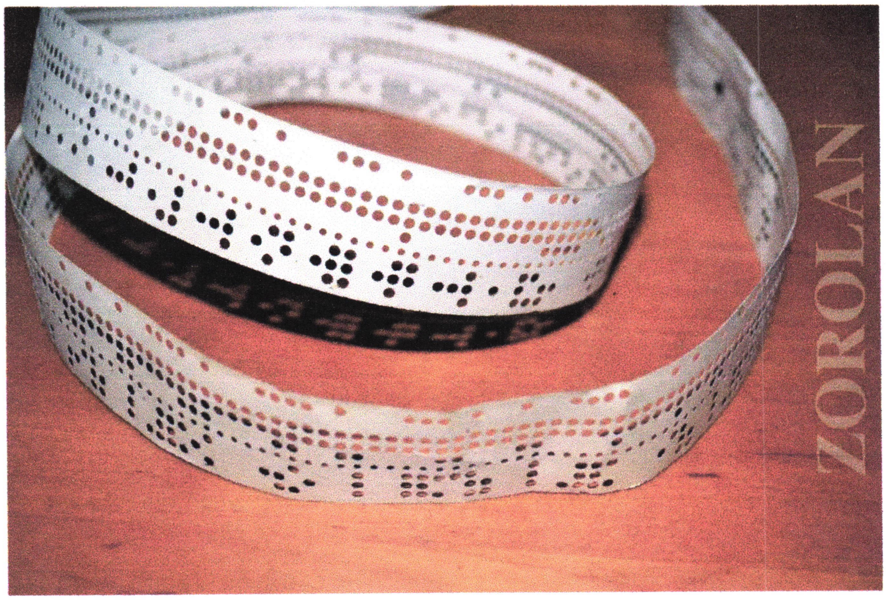


Figure 5-2. Simulation - Control ROM Listing



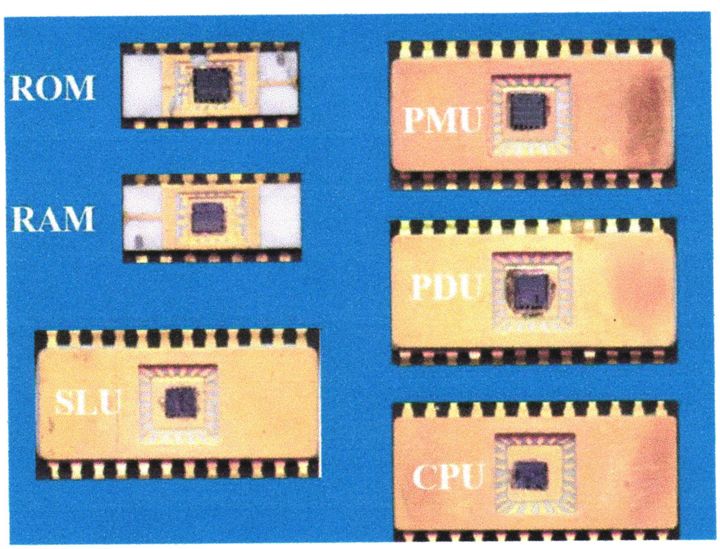
5. Submit the binary 1's and 0's patterns to AMI to manufacture the Read-Only Memory chips. The 1's and 0's had to be submitted in the form of a rolled paper tape. This was before the Internet, hard drive, floppy drive, or any other electronic form of storage. Paper tape was it. Two years work resulted to 1000's of holes on a paper tape.

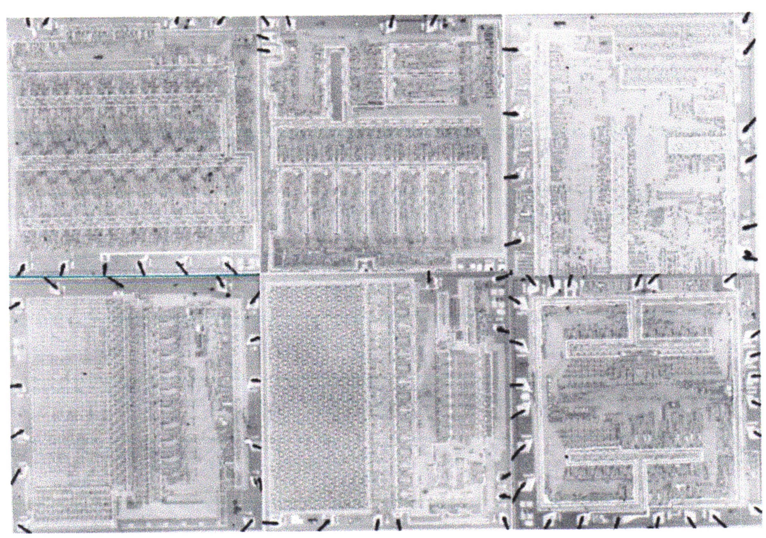


Next, we waited 2-3 months for the first set of chips to be manufactured. In reality, there were endless possibilities of things going wrong. However, the first set of chips worked perfectly. No celebration. Excellence and perfection were expected from a military engineering environment. Life goes on and the F14 saved the days ... at least in the movies and in Desert Storm. 😊

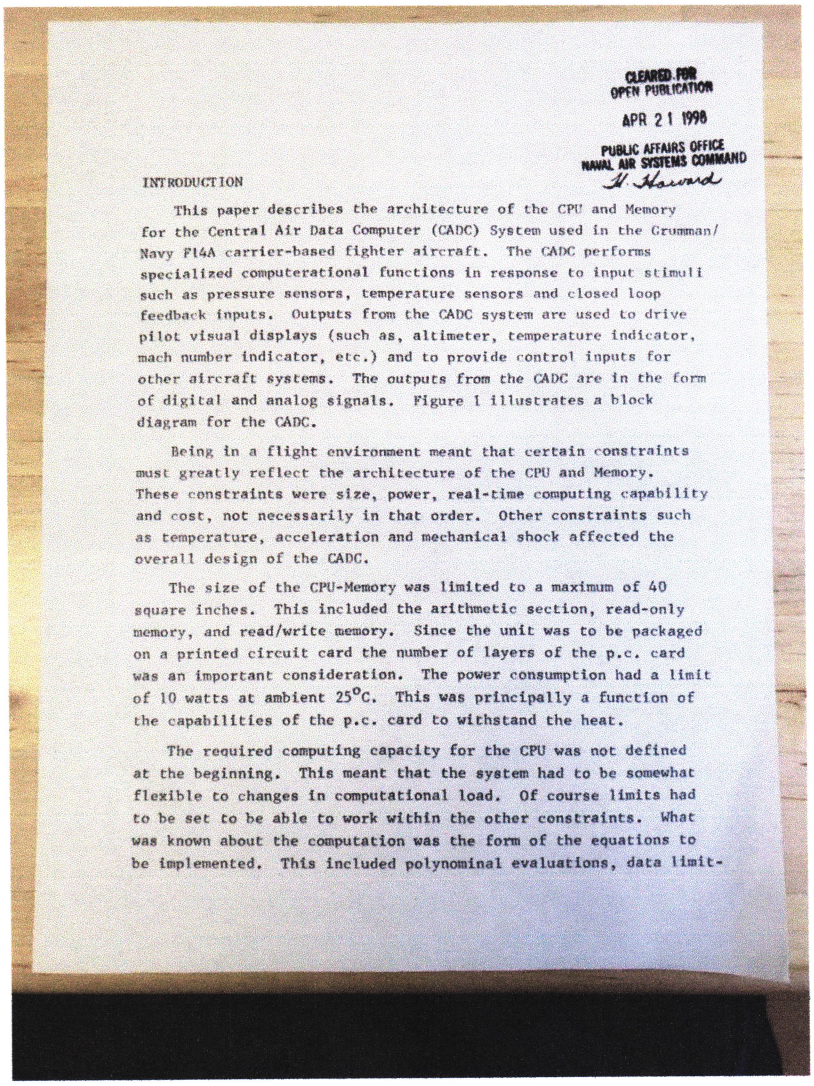
Left: Six different packaged chip types make the microprocessor. This is the first set off the production line that worked the first time. Circa: March 1970

Right: Photos of the microchips inside the packaging.





Left: First page of my paper that I could not publish in Computer Design Magazine in 1970. Paper never published.
Right: US Navy stamp clearing me to discuss the paper and the project. April 21, 1998.



CLEARED FOR
OPEN PUBLICATION

APR 2 1 1998

PUBLIC AFFAIRS OFFICE
NAVAL AIR SYSTEMS COMMAND
H. Howard

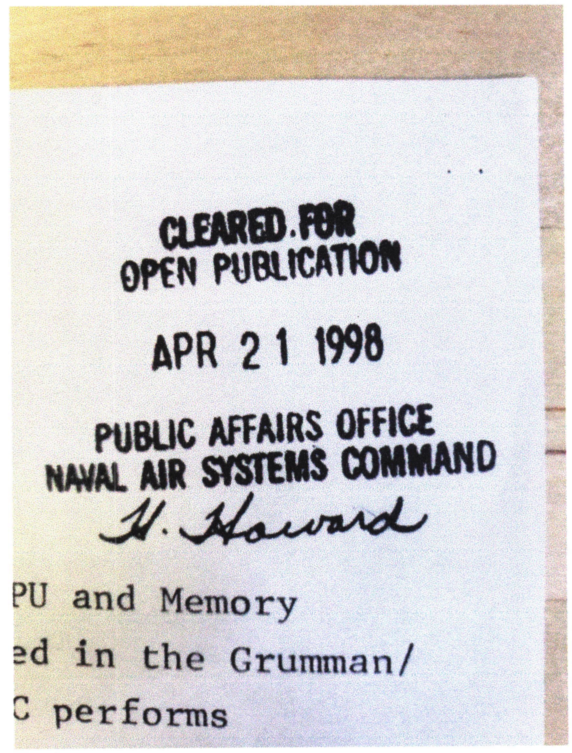
INTRODUCTION

This paper describes the architecture of the CPU and Memory for the Central Air Data Computer (CADC) System used in the Grumman/ Navy F14A carrier-based fighter aircraft. The CADC performs specialized computerational functions in response to input stimuli such as pressure sensors, temperature sensors and closed loop feedback inputs. Outputs from the CADC system are used to drive pilot visual displays (such as, altimeter, temperature indicator, mach number indicator, etc.) and to provide control inputs for other aircraft systems. The outputs from the CADC are in the form of digital and analog signals. Figure 1 illustrates a block diagram for the CADC.

Being in a flight environment meant that certain constraints must greatly reflect the architecture of the CPU and Memory. These constraints were size, power, real-time computing capability and cost, not necessarily in that order. Other constraints such as temperature, acceleration and mechanical shock affected the overall design of the CADC.

The size of the CPU-Memory was limited to a maximum of 40 square inches. This included the arithmetic section, read-only memory, and read/write memory. Since the unit was to be packaged on a printed circuit card the number of layers of the p.c. card was an important consideration. The power consumption had a limit of 10 watts at ambient 25°C. This was principally a function of the capabilities of the p.c. card to withstand the heat.

The required computing capacity for the CPU was not defined at the beginning. This meant that the system had to be somewhat flexible to changes in computational load. Of course limits had to be set to be able to work within the other constraints. What was known about the computation was the form of the equations to be implemented. This included polynominal evaluations, data limit-



First F14 flight Dec 1970