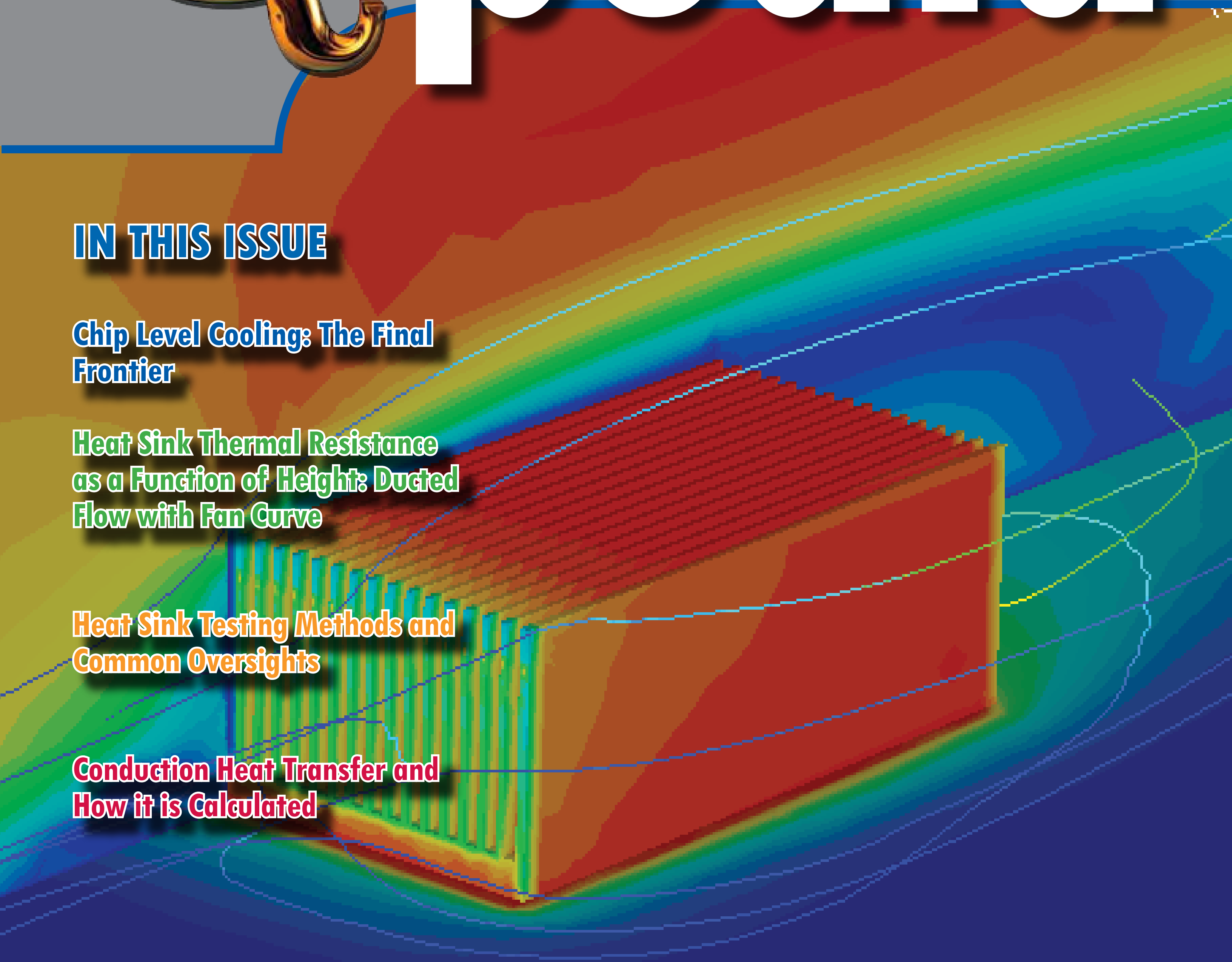
JANUARY 2009 | VOLUME II | ISSUE XII

Qpedia



IN THIS ISSUE

Qpedia

SUBSCRIBE ON LINE AT:
www.qats.com/qpedia

Advanced Thermal Solutions is a leading engineering and manufacturing company supplying complete thermal and mechanical packaging solutions from analysis and testing to final production. ATS provides a wide range of air and liquid cooling solutions, laboratory-quality thermal instrumentation, along with thermal design consulting services and training. Each article within Qpedia is meticulously researched and written by ATS' engineering staff and contributing partners. For more information about Advanced Thermal Solutions, Inc., please visit www.qats.com or call 781-769-2800.

EDITOR
KAVEH AZAR, Ph.D.
President & CEO,
Advanced Thermal Solutions, Inc.

MANAGING EDITOR
BAHMAN TAVASSOLI, Ph.D.
Chief Technology Officer,
Advanced Thermal Solutions, Inc.

NORTH AMERICA
ADVANCED THERMAL SOLUTIONS, INC.
89-27 Access Road Norwood, MA 02062 USA
T: 781.769.2800 | F: 781.769.9979 | www.qats.com

EUROPE
ADVANCED THERMAL SOLUTIONS, B.V.
De Nieuwe Vaart 50 | 1401 GS Bussum
The Netherlands
T: +31 (0) 3569 84715 | F: +31 (0) 3569 21294
www.qats-europe.com

ADVERTISING
TO PLACE AN AD IN QPEDIA:

Contact Ray Santos at 781.769.2800

Qpedia was launched in 2007 as a technology eMagazine focused on the thermal management of electronics. It is designed as a resource to help the engineering community solve the most challenging thermal problems.

The eMagazine is published monthly and distributed at no charge to over 21,000 engineers worldwide. Qpedia is also available online or for download at www.qats.com/qpedia.

Qpedia's editorial team includes ATS' President & CEO, Kaveh Azar, Ph.D., and Bahman Tavassoli, Ph.D., the company's chief technologist. Both Azar and Tavassoli are internationally recognized experts in the thermal management of electronics.

For more information on how you can generate awareness about your company or products, contact Ray Santos at 781.769.2800.

Features

Thermal Management Design Kit

ATS-TMDK-96

ATS ADVANCED THERMAL SOLUTIONS, INC.
Innovations in Thermal Management®

Advanced Thermal Solutions' Thermal Management Design Kit contains 96 of its best-selling maxiFLOW™ heat sinks and maxiGRIP™ sink attachment systems, to quickly provide optimum component cooling solutions during the prototyping, trouble shooting and final design stages.

There are 288 parts in all, including heat sink, frame clip, spring clip and pre-applied thermal interface material for 16 of the most common component sizes available. This allows engineers to have the best cooling solution available for nearly every application.

ATS maxiFLOW heat sinks feature a low profile, spread fin array to maximize surface area for more effective air (convective) cooling. The maxiGRIP heat sink attachment system features a plastic frame clip and a stainless steel spring clip that runs through the heat sink's fin field, fastens securely to the plastic frame and applies steady, even pressure to the component throughout the product lifecycle.

Every heat sink in the Kit comes with a high quality thermal interface material to enhance cooling performance and allow immediate qualification testing. An enclosed catalog provides each heat sink's part number, dimensions (base and fin tip to fin tip) and cooling performance in both ducted and unducted airflow conditions.

All parts in the kit are RoHS compliant.

Individual orders of maxiFLOW heat sinks with maxiGRIP frame and spring clip assemblies, including replacements for the Kits, are available exclusively from Digi-Key, and can be ordered at digikey.com. Tools that aid in the installation and removal of the assemblies are also available and can be ordered from Digi-Key or ATS.

COMPONENT SIZES:

17 mm x 17 mm
19 mm x 19 mm
21 mm x 21 mm
23 mm x 23 mm
25 mm x 25 mm
27 mm x 27 mm
29 mm x 29 mm
30 mm x 30 mm
31 mm x 31 mm
32.5 mm x 32.5 mm
33 mm x 33 mm
35 mm x 35 mm
37.5 mm 37.5 mm
40 mm x 40 mm
42.5 mm x 42.5 mm
45 mm x 45 mm

COMPONENT HEIGHTS:

Standard - 3 mm to 4.5 mm
Low Profile - 1.5 mm to 2.99 mm

HEAT SINK HEIGHTS:

STD	LP
7.5 mm	9.5 mm
12.5 mm	14.5 mm
17.5 mm	19.5 mm

» **96 Heat Sink Assemblies**
Each includes a heat sink, with pre-applied phase-changing thermal interface material, plastic frame clip and stainless steel spring clip

» **Ideal for Prototyping & Testing**
Allows engineers to have the best cooling solution available for nearly every application

» **Parts Available from Digi-Key**
Additional samples and replacement parts are conveniently available from Digi-Key and can be ordered at www.digikey.com

» **maxiFLOW™ Heat Sinks**
maxiFLOW heat sinks reduce device junction temperatures (T_J) by more than 20 percent, compared with other heat sinks of comparable volume

» **maxiGRIP™ Attachment**
Provides secure heat sink attachment and applies steady, even pressure to the component throughout the product lifecyle

» **Meets Shock & Vibration Standards**
maxiGRIP assemblies are certified to meet Telcordia, ETSI and MIL-STD vibration and shock test standards

» **Detailed Performance Data**
An enclosed catalog provides each heat sink's part number, dimensions (base and fin tip to fin tip) and cooling performance in both ducted and unducted airflow conditions.

» **RoHS Compliant**

For further technical information, please contact Advanced Thermal Solutions, Inc. at 1-781-769-2800 or www.qats.com

89-27 ACCESS ROAD, NORWOOD, MA 02062 USA | T: 781.769. 2800 F: 781.769.9979 | WWW.QATS.COM

Chip Level Cooling

The Final Frontier

With clock rates and transistor counts increasing in today's microprocessors, power dissipation has become a critical part of system design complexity. Thermal and power delivery issues are especially significant in high performance computing systems. As device densities and clock frequencies continue to increase, the switching currents carried by the power and ground networks increase as well, leading to an increase in power density. This increase, along with the lower power supply voltages and thinner wires, can adversely affect the robustness of the IC. Power distribution systems are designed to provide needed voltages and currents to the transistors that perform the logic functions of a chip. The supply voltages are assumed to be constant across a chip, and are expected to operate reliably over the chip's lifetime. The complexity of power distribution systems and their subsequent spot heating have a significant impact on chip performance. If IC designers do not consider such matters, they will have a difficult time producing a robust system since the chip can fail in the field after it is embedded in a system.

This issue is acutely highlighted by ITRS: Table 1 shows the trends in electronics packaging for the next eleven years [1].

Table 1. High Performance Logic Technology Trend Targets [1].

Year	2007	2010	2013	2016	2019
	Planar Bulk		Double Gate		
Supply Voltage (V)	1.1	1.0	0.9	0.8	0.7
[1]Transistor (M)	1106	2212	4424	8848	17696
[2]Size (mm^2)	310	310	310	310	310
[3]L_g (nm)	25	18	13	9	6
[4]$I_{d.sat}$ (uA/um)	1200	2050	2220	2713	2744
[5]$I_{sd,\ leakage}$ (uA/um)	0.2	0.28	0.11	0.11	0.11
[6]Intrinsic Delay, τ (ps)	0.64	0.40	0.25	0.15	0.10
[7]Switching Energy (fJ)	0.1634	0.0447	0.0198	0.0091	0.0036
[8]Max, P.D.(W/cm^2)	60.97	63.87	63.87	63.8	63.87

[1]Functions per chip at production (million transistors)
[2]Chip size at production (mm^2)
[3]Physical gate length (nm)
[4]Effective saturation drive current (uA/um)
[5]Source/drain sub-threshold off-state leakage current (uA/um)
[6]Intrinsic transistor delay for NMOS devices at 25^0C (ps)
[7]Energy per device switching transition with dimensions $W/L_g=3$ (fJ/device)
[8] Maximum allowable average power density (W/cm^2)

As observed by Lin, et al., [2], the projected allowable maximum power density (shown in Table 1) is approaching saturation in the next few years, due to the limited capability for system level heat removal. While increasing the chip size can reduce the overall heat flux, the desire to place more circuitry on the same silicon will negate the notion of a larger chip. As noted by Taur [3], the thermal problems are amplified because the leakage current (power at the transistor level) forms the major portion of the total power dissipated by the chip. Concluding this leakage is undesirable from the thermal stand point, it has become the primary factor in limiting the scaling of CMOS devices.

As the power dissipation across the chip has risen, the local so-called, “hot-spots” have become a unique challenge for device designers and thermal engineers. As a result of the combination of small device features and passage of electrical current in such locations, the local heat flux densities have risen dramatically while posing a significant challenge for cooling thermal spikes on the chip. Figure 1 shows one such effect where there is significant power and subsequently temperature distribution on the chip, [4]

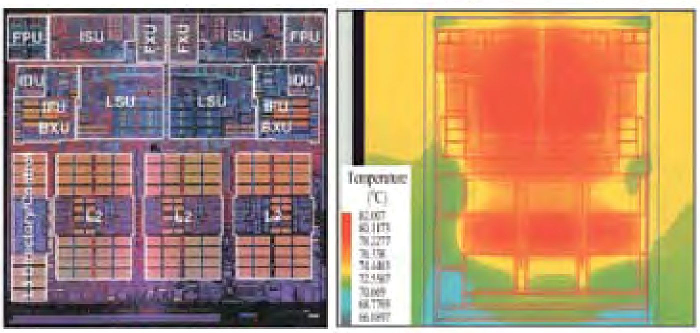


Figure 1. Map of FET Junction Temperature for a 115 W Packaged Power 4 Chip Derived from Chip Power Analysis and Thermal Modeling Simulation [4].

The power profile over the chip has peaks and valleys, whereby the peaks represent the highest power concentration (largest heat flux, W/mm^2) and highest temperature levels on the chip. This is depicted in Figure 2 for a CPU.

These peaks have a proportionally higher temperature than the rest of the chip and represent the potential for a chip's malfunction or its catastrophic failure. Once we translate this to a PCB, some of the components are of high to average power and some are of low to average power. Consequently, the PCB has the same power and thermal response as the chips on the components forming the PCB. This impacts the thermal response of the components residing on it, i.e., change of boundary conditions. The thermal management at both levels of packaging, chip (component) and PCB, are huge bottlenecks in the successful launch of an application. They become even more prevalent as the heat flux density increases.

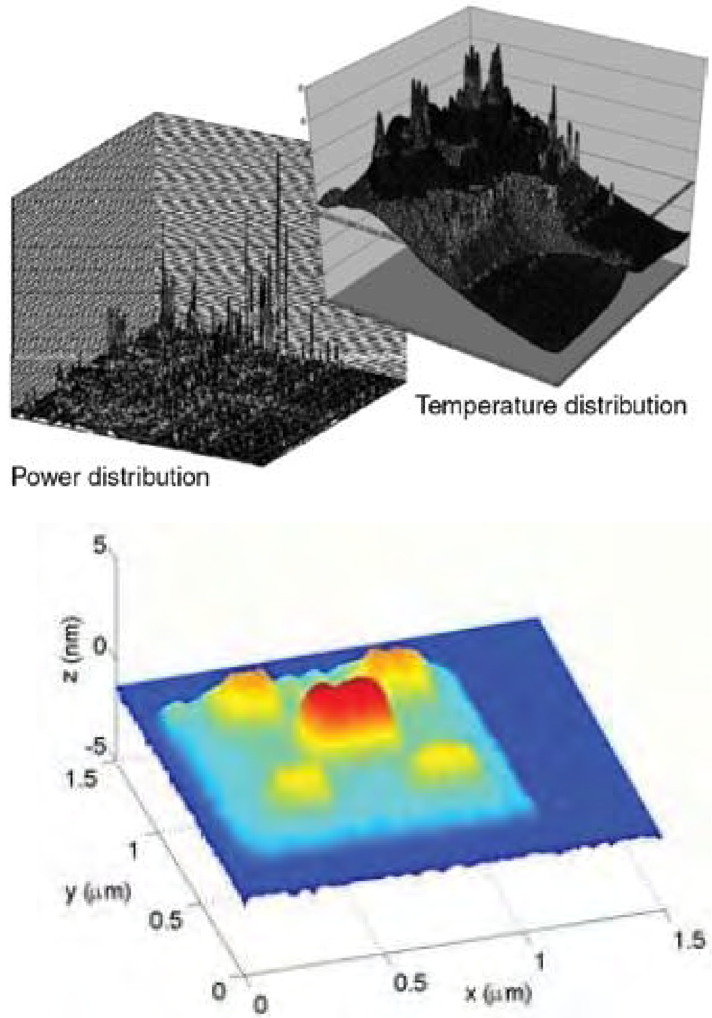


Figure 2. Power and Temperature Distributions at the CPU Junction [5].

Despite significant advances in component packaging and material-design, the industry continues to struggle with this issue. The solution for the spot cooling has two broad forms –

- At the silicon level
- At the package level.

Silicon Level

At the silicon level, a number of solutions have been explored. These include: deployment of Micro-Channel Heat Exchanger (MCHE), Thin Film Thermo Electric Cooler, Micro-Heat Pipes or Localized Copper bumps to facilitate the spreading of the heat on a larger surface area or transporting it to a different location in the case of MCHE. Figure 3 shows a stacked MCHE

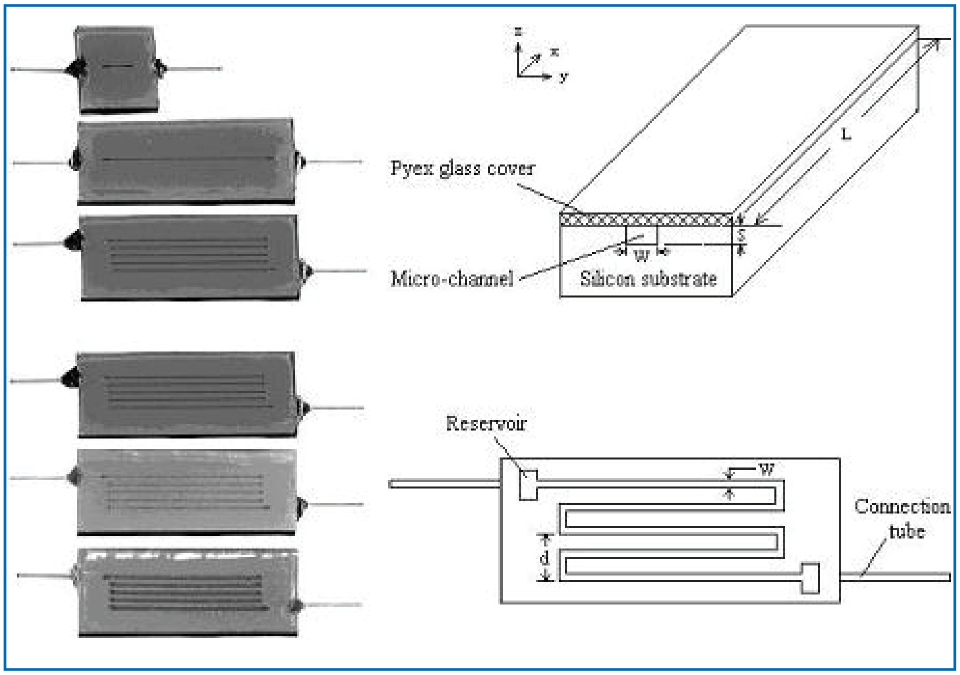


Figure 3. Stacked Micro Channel Heat Exchanger for Substrate Cooling [6].

that is used for cooling a silicon substrate.

The success of these techniques (except for a handful of highly customized applications, such as larger scale computers) has been weak and unsatisfactory. The TEC, Bump, micro heat pipes, etc, have had moderate success in dampening the peaks observed as a result of the power density variation. Often, because of the aspect ratio or the area, the heat flux exceeds 400-500 W/cm^2. In some high power applications, it exceeds 1-2 kW/cm^2. With such high heat fluxes, one can appreciate the limits of the aforementioned technologies.

An interesting approach to this problem, apart from the mainstream thermal sciences, has been the electrical control of the chip, which is highlighted in [7]. In this technique, named, Dynamic Thermal Management (DTM) for High-Performance Microprocessors, the authors have investigated the dynamic thermal management as a technique to control CPU power dissipation. As stated in their paper, the term Dynamic Thermal Management refers to a range of possible hardware and software strategies which work dynamically, at run-time, to control a chip's operating temperature. Traditionally, the packaging and fans for a CPU or computer system are designed to be able to maintain a safe operating temperature even when the chip was dissipating the maximum power possible for a sustained period of time, and therefore generating the highest amount of thermal energy. This worst-case thermal scenario is highly unlikely, however, and thus such worst-case packaging is often expensive overkill. DTM allows packaging engineers to design systems for a target sustained thermal value that is much closer to average-case for real benchmarks. If a particular workload operates above this point for sustained periods, a DTM response will work to reduce chip temperature. In essence, DTM allows designers to focus on average, rather than worst-case, thermal conditions in their designs.

The key goals of DTM can be stated as follows:

1. to provide inexpensive hardware or software responses,
2. to reliably reduce power and,
3. to impact performance as little as possible."

To better understand the process the authors state that "the maximum power dissipation occurs when all of the structures within the processor are active with maximum switching activity. In reality, the maximum power dissipation is constrained by the software program that can maximize the usage and switching activity of the hardware. Special max-power benchmarks can be written to maximize the switching activity of the processor. These benchmarks are often quite esoteric, perform no meaningful computation, and dissipate higher power than "real" programs. Thus, DTM techniques could be used solely to target power levels seen in maximum power benchmarks and would rarely be invoked during the course of typical applications." As depicted in Figure 4, there are three horizontal dashed lines. The topmost line shows the designed for cooling capacity of the machine without DTM. The second line shows that the cooling capacity could be reduced if dynamic techniques were implemented, because DTM reduces the effective maximum power dissipation of the machine. Finally, the lowest horizontal line shows the DTM trigger level. This is the temperature at which the DTM techniques are engaged.

Two curves in Figure 4 show chip temperature for some sequence of code being executed on the machine.The upper, solid curve is executed on the machine without DTM, and the lower, dotted curve is executed on a machine that has implemented DTM. Both curves are the same until the DTM trigger level is exceeded. At this point, after a small delay to engage the response, the curves diverge. In the uppermost curve the chip temperature slowly increases and then falls back below the trigger level. The lower curve shows how DTM would affect the same sequence of code.

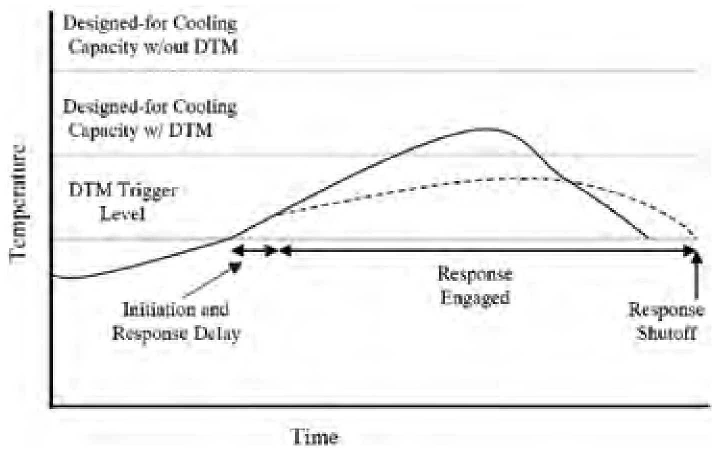


Figure 4. Overview of the Dynamic Thermal Management (DTM) Technique [7].

Package Level

At the package level, the cooling solutions can be applied to the top of the silicon, or alternatively the component is immersed in some sort of heat transfer fluid. The goal of these approaches is to rapidly remove the heat from the device or to provide a medium that can effectively absorb the thermal peaks by improved thermal spreading. A number of techniques have been explored by many researchers in the field with varied success. Reference [8] provides a detailed review of different techniques, highlighting their salient features and challenges for deployment. Table 2 presents such techniques and their respective characteristics.

Table 2. Thermal and Deployment Characteristics of Select Cooling Options, [8].

Technology	Advantages	Disadvantages
Fan sinks = heat pipe (hybrid	Compact, versatile	Reliability, space, limited to ambient temperature
Thermoelectric	Spot cooling	Reliability, low capacity
Liquid cooling	High surface heat transfer	Sealing, cost, maintenance, packaging
Direct immersion	High capacity	Cost, sealing, packaging
Refrigeration	Sub-ambient	Cost, power, space, packaging
Cryogenics	Super cooling	Cost, power, packaging

Other researchers have highlighted the other cooling solutions that are deployed or exist at university or company laboratories, [9 and 10]. In an excellent paper by Lin and Banerjee [2] the authors demonstrate the impact of the global and local cooling solution as is applied to hot spots on dies specifically designed for such study.

Figure 5a and 5b show the functional block layout of a test chip showing power density associated with each block. Nominal total power consumption is 90 W, and Figure 5b shows four hot-spots on the topical substrate temperature profile of the test chip. In this case, the highest temperature is around 73 °C.

And Figure 6a and 6b show the topical substrate temperature profile of the test chip for global and spot cooling respectively.

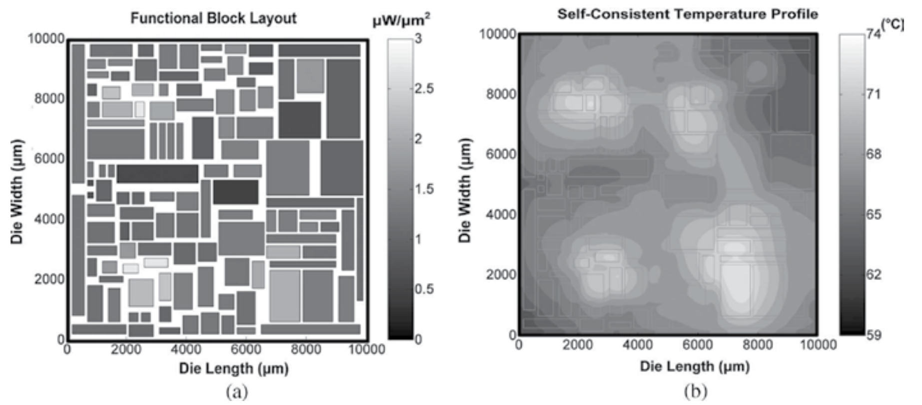


Figure 5. Block Diagram and the Topical Temperature Measurement of a 10 x 10 mm Test Chip, respectively [11].

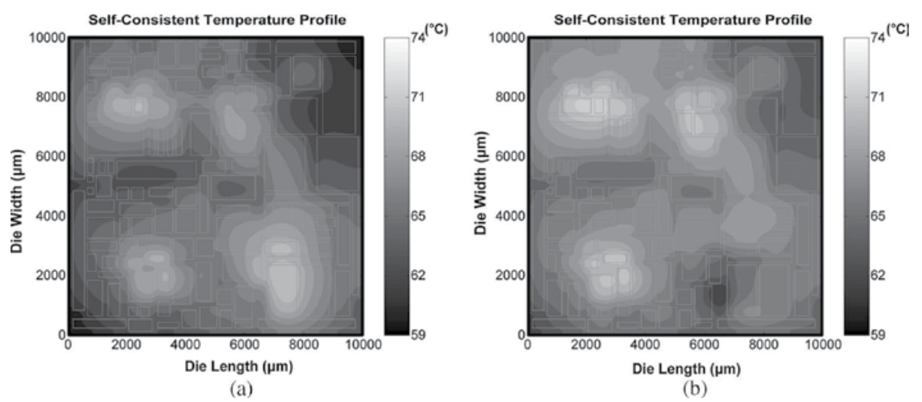


Figure 6. Topical Temperature Difference for Global (6a) and Spot Cooling (6b) of a 10 x 10mm Test Chip.

As stated by the authors, “the substrate temperature profile, (Figure 5b), shows several hot spots and the highest junction temperature is around 73 °C. Although the results shown here are specific to the aforementioned IC, the conclusions drawn are more generic. Figure 6 shows the effect of applying global and localized cooling strategies on hot spot management. As shown in Figure 6a, a lower junction-to-ambient thermal resistance (θ_{ja}) obtained by applying global cooling (through better interface material, higher cooling efficiency, etc.) reduces the maximum junction temperature. However, on-chip hot spots and thermal gradients still remain. On the other hand, localized cooling solutions such as local spray cooling and thin-film thermoelectric coolers can be applied to eliminate the hot spots. For example, if a thin-film thermoelectric cooler is placed on the backside of the wafer below the location of the bottom-right hot spot, it can effectively eliminate the targeted hot spot as shown in Figure 6b.”

Summary

The power profile over the chip has peaks and valleys. The peaks represent the highest power concentration (largest heat flux, W/mm^2) and highest temperature levels on the chip. Thermal management of the so-called hot-spots has become a unique challenge for device designers and thermal engineers alike. Through the combination of smaller device features and the passage of electrical current in such locations, local heat flux densities have risen dramatically. They pose a significant challenge for cooling thermal spikes on the chip.

To successfully manage such occurrences, it is clear that a topical or spot approach for thermal management of these hot spots alone is not sufficient. To successfully develop such products, it is essential for thermal management and logic-flow to be considered concurrently, and for a system level approach for cooling to be taken.

References

1. International Technology Roadmap for Semiconductors (ITRS). www.itrs.net.
2. Lin, S. and Banerjee, K., Cool Chips: Opportunities and Implications for Power and Thermal Management, IEEE Transactions On Electron Devices, Vol. 55, No. 1, January 2008.
3. Taur, Y., CMOS Design Near the Limit of Scaling, IBM J. Res. Develop., Vol. 46, No. 2/3, 2002
4. Warnock, J., Keaty, J.,Petrovick, J., Clabes, J., Kircher, C., Krauter, B., Restle, P. Zoric, B..and Anderson, C., The Circuit and Physical Design of the POWER4 Microprocessor, IBM Journal of Research and Development, Vol. 46, No. 1, 2002.
5. Wei, J., Thermal Management of Fujitsu’s High-Performance Servers, Fujitsu Sci. Tech. J., 43, January 2007.
6. Web Reference : http://plaza.ufl.edu/rxiong/research/ST-flow_files/micro-channels.JPG
7. Brooks, D. and Martonosi, M., Dynamic Thermal Management for High-Performance Microprocessors, Proceedings of the 7th International Symposium on High-Performance Computer Architecture, Monterrey, Mexico, January 2001.
8. Azar, K., Advanced Cooling Concepts and Their Challenges, Presented at the Int. Workshop Thermal Investigations ICs and Systems (THERMINIC), Madrid, Spain, 2002.
9. Rodgers, P., Eveloy, V., and Pecht, M.,Limits of Air-Cooling: Status and Challenges, Proc. SEMI-THERM, 2005.
10. Prasher, R., Chang, J., Sauciuc, I., Narasimhan, S., Chau, D., Chrysler, G., Myers, A., Prstic, S., and Hu, C., Nano and Micro Technology-Based Next-Generation Package-Level Cooling Solutions, Intel Technol. J., Vol. 9, No. 4, November 2005.

Heat Sink Thermal Resistance

As a Function of Height: Ducted Flow with Fan Curve

In the October 2008 issue of Qpedia, we looked at the thermal performance of a heat sink as a function of height for a ducted flow, but with a fixed volumetric flow rate. This implies that we have a constant pressure source of airflow that is independent of the pressure drop caused by the heat sink [1]. Another article considered thermal performance as function of the number of fins for a ducted flow, but with a fan curve involved [2]. Here, we look at the performance of a heat sink as a function of height, but in a real case scenario with a fan curve involved. The heat sink geometry and size are exactly the same as in the earlier issue. Figure 1 shows the front view of a simple straight heat sink.

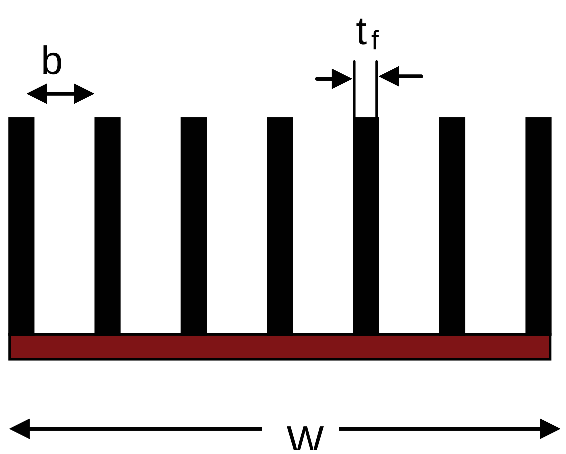


Figure 1. Schematic of a Simple Straight Fin Heat Sink.

Where,

b = fin-to-fin spacing

t_f = fin thickness

H = fin height

W = width of the heat sink

The heat sink thermal resistance (R_{sa}) is defined by the following equation [1],

$$R_{sa} = \frac{1}{\eta h A_{fin}} + \frac{1}{2\dot{m}C_p} \qquad (1)$$

Where,

R_{sa} = sink-to-ambient thermal resistance

h = heat transfer coefficient

A_{fin} = heat sink fin area + base area between fins

$\dot{m}$ = mass flow rate, equal to $\rho V_f A$

V_f = velocity between fins

A = total cross sectional area of the channels between fins

C_p = specific heat at constant pressure

To determine $R_{sa,}$ the heat transfer coefficient (h) and flow velocity within the fin field (V_f) must be determined. In Equation 1, the heat transfer coefficient is based on the average air temperature between the fins. The second term is included for the additional thermal resistance of the fluid due to its thermal capacitance. If we base the heat transfer coefficient on the inlet air temperature, the heat transfer coefficient is obtained from Equation 2 [2]:

$$Nu_b = \left[\frac{1}{\left(\frac{R_e \cdot Pr}{2}\right)^3} + \frac{1}{\left(0.664 Re^{1/2} Pr^{0.33} \sqrt{1 + \frac{3.65}{R_e^{1/2}}}\right)^3} \right]^{-0.33} \qquad (2)$$

Where,

Nu_b = hb/k

K = fluid thermal conductivity

R_e = Reynolds number, equal to $\rho V_f b^2/\mu L$
B = fin-to-fin spacing
μ = dynamic viscosity
L = heat sink length
By using the above heat transfer coefficient, the second term in Equation 1 drops and the heat sink thermal resistance is calculated from:

$$R_{sa} = \frac{1}{\eta h A_{fin}} \qquad (3)$$

The pressure drop is calculated as follows [3]:

$$\Delta P = (K_c + 4f_{app} \cdot \frac{L}{D_h} + K_e) . \rho \frac{V_f^2}{2} \qquad (4)$$

Where,
ρ = density
D_h = hydraulic diameter
The other terms are defined as follows:
K_e and K_c are pressure loss coefficients for sudden expansion and contraction [3], respectively, and are defined as,

$$\begin{aligned} K_c &= 0.42.(1-\sigma^2) \\ K_e &= (1-\sigma^2)^2 \end{aligned} \qquad (5)$$

Where,
σ = the ratio of the open channel area to the total frontal area
f_{app} = the apparent friction factor for hydrodynamically developing laminar flow

$$f_{app} = \frac{\left[\left(\frac{11.8}{L^*}\right) + (f.Re)^2 \right]^{1/2}}{Re} \qquad (6)$$

Where,

$$L^* = \frac{L/D_h}{Re} \qquad (7)$$

and L = heat sink length in the direction of the flow
The Reynolds number is defined differently than the Nusselt number calculation and is defined as,

$$Re = \frac{\rho . V_f . D_h}{\mu} \qquad (8)$$

f is the friction factor for a fully developed laminar flow and is defined as,

$$f = (24 - 32.53 \cdot \lambda + 46.72 \cdot \lambda^2 - 40.83 \cdot \lambda^3 + 22.96 \cdot \lambda^4 - 6.09 \cdot \lambda^5)/Re \qquad (9)$$

Where the aspect ratio is defined as,

$$\lambda = \frac{b}{H} \qquad (10)$$

Let's consider a heat sink with the following characteristics.

Width = 80 mm
Length = 80 mm
Base thickness = 4 mm
Height = 30 mm (variable)
Fin thickness = 0.5 mm
Number of fins = variable
Let's assume we are using a fan with the characteristics in Table 1:

Table 1. Fan Characteristic Assuming a Linear Curve.

Pressure	Volumetric Flow Rate
0	0.0148 m^3/sec (33 CFM)
650 Pa (2.6 H2O")	0

In the first scenario, we assume that the flow is fixed at 0.0148 m^3/sec and the pressure drop has no effect on the fan flow rate. We also assume that the heat source is 80 x 80 mm, so there is no spreading resistance. The number of fins is fixed at 60 for all subsequent cases.

Figure 2 shows the thermal resistance of this heat sink as a function of height when it varies from 10 to 30 mm. The graph shows that the rate of improvement of the thermal resistance decreases as the height, increases. In fact, after reaching a height of 25 mm, the improvement in performance has almost reached a practical asymptote. Figure 3 shows that the pressure drop in the heat sink decreases as the fin height increases. This is due to the fact that, with taller fins, the larger aspect ratio channels formed between the fins create less pressure drop compared to shorter fins with a smaller channel aspect ratio. The results also show that taller fins create slower airflow velocity, hence less pressure drop..

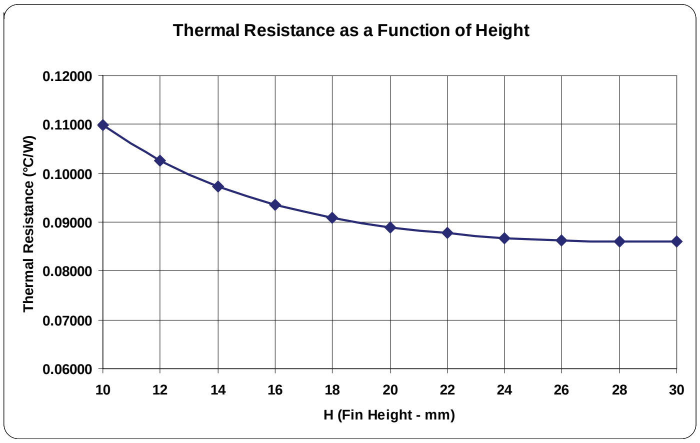


Figure 2. Thermal Resistance of the 80 x 80 mm Heat Sink as a Function of Fin Height For a Ducted Flow-Fixed Flow.

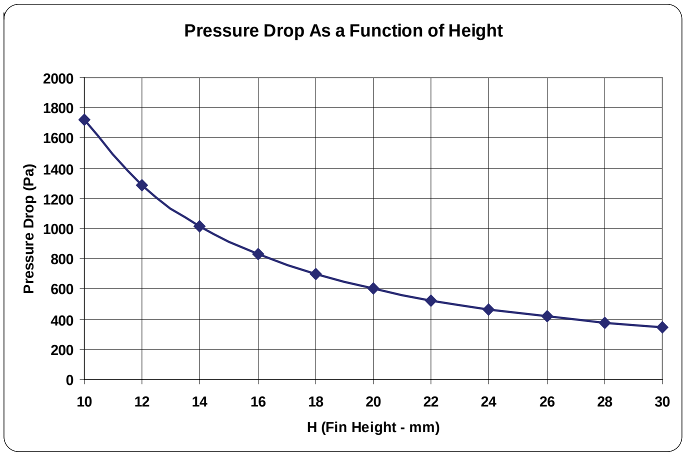


Figure 3. Pressure Drop of the 80 x 80 mm Heat Sink as a Function of Fin Height for a Ducted Flow-Fixed Flow.

The above graphs are based on a hypothetical fixed flow. Now, let's consider a real life situation with the above specified fan. For simplicity, we assume the fan curve is a straight line. In order to calculate the thermal resistance of the heat sink, we must first know how much airflow is provided to the heat sink by the fan. This is found by intersecting the heat sink pressure curve and the fan curve. The point of intersection is the operating point of the system, which determines the volumetric flow rate and, hence, the thermal resistance. Figure 4 shows the fan and the heat sink curves for fin heights ranging from 10 to 30 mm. It can be seen that by increasing the fin height, the heat sink curve shifts downward and the operating point – the intersection of the fan curve and the heat sink curve – moves to the right hand side on the X axis (volumetric flow rate axis), thus increasing the volumetric flow rate. Figure 5 shows the thermal resistance of the heat sink as a function of fin height. This figure demonstrates that as we increase the fin height, the thermal resistance continuously decreases. The interesting observation from this graph is that the thermal resistance does not reach an asymptote. The reasons for this continuous improvement in performance are the decrease in pressure drop, increase in volumetric flow rate and increase in surface area. Figure 6 compares the two cases of fixed flow and flow with a fan curve. This graph shows that the difference in thermal performance between the two cases decreases as the fin height increases.

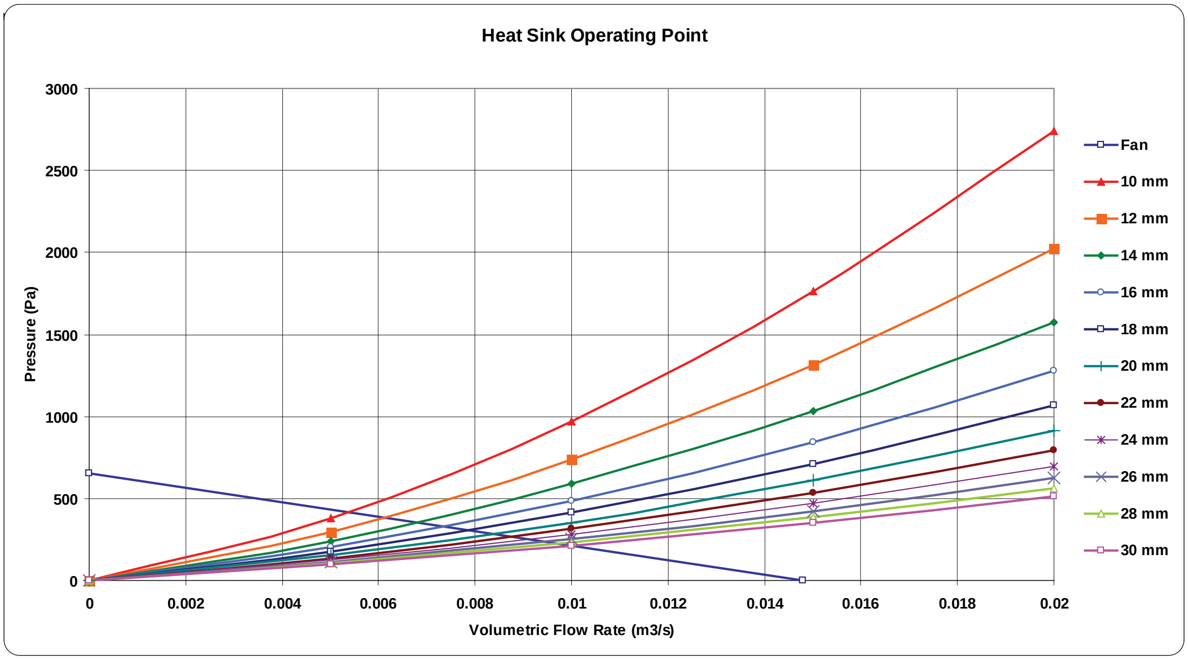


Fig 4. Fan Curve and the 80 x 80 mm Heat Sink Pressure Drop for Different Fin Heights.

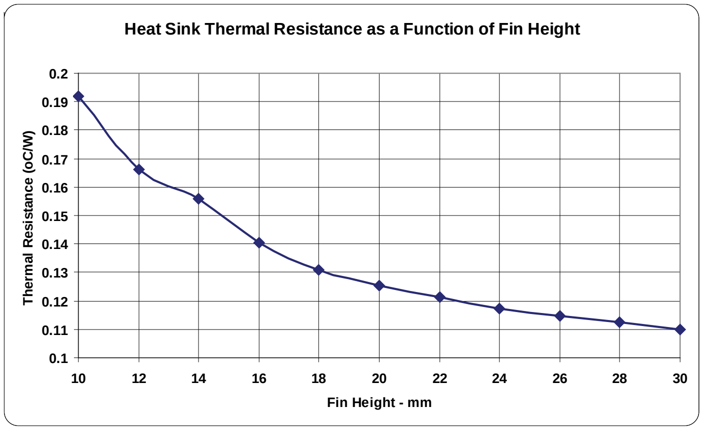


Figure 5. Thermal Resistance of the 80 x 80 mm Heat Sink as a Function of Number of Fins.

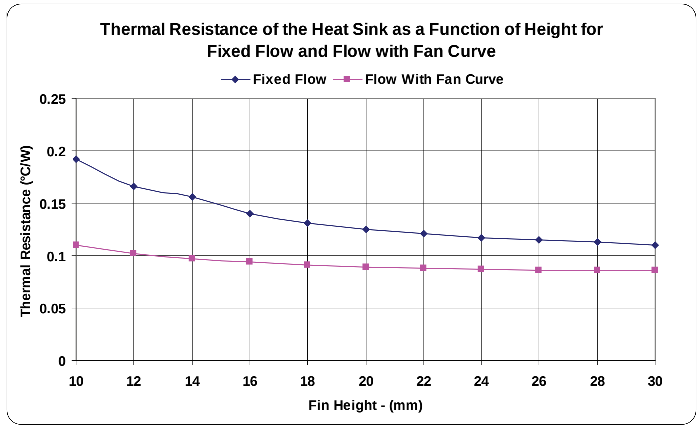


Figure 6. Thermal Resistance of the Sink as a Function of Fin Height for Two Cases of Fixed and Flow with Fan Curve

There are few choices for increasing the performance of the heat sink. Some of the options are to select a fan with higher pressure, higher flow rate, fans in series, or fans in parallel. In any of these cases the fan and heat sink curves should be plotted, repeat the above process to find the operating point and follow the trend. Figure 7 shows the same heat sink pressure curves along with pressure curves for two fans either in parallel or in series. The combination to use depends on the fin height. Point A is the intersection between the two curves for series and parallel combination. Figure 7 shows that if we are on the right hand side of point A, parallel combination will provide more flow. On the other hand, if we are on the left hand side of point A, a series combination is better. This implies if the fin height is more than 16 mm we use a parallel combination, otherwise we use the series combination.

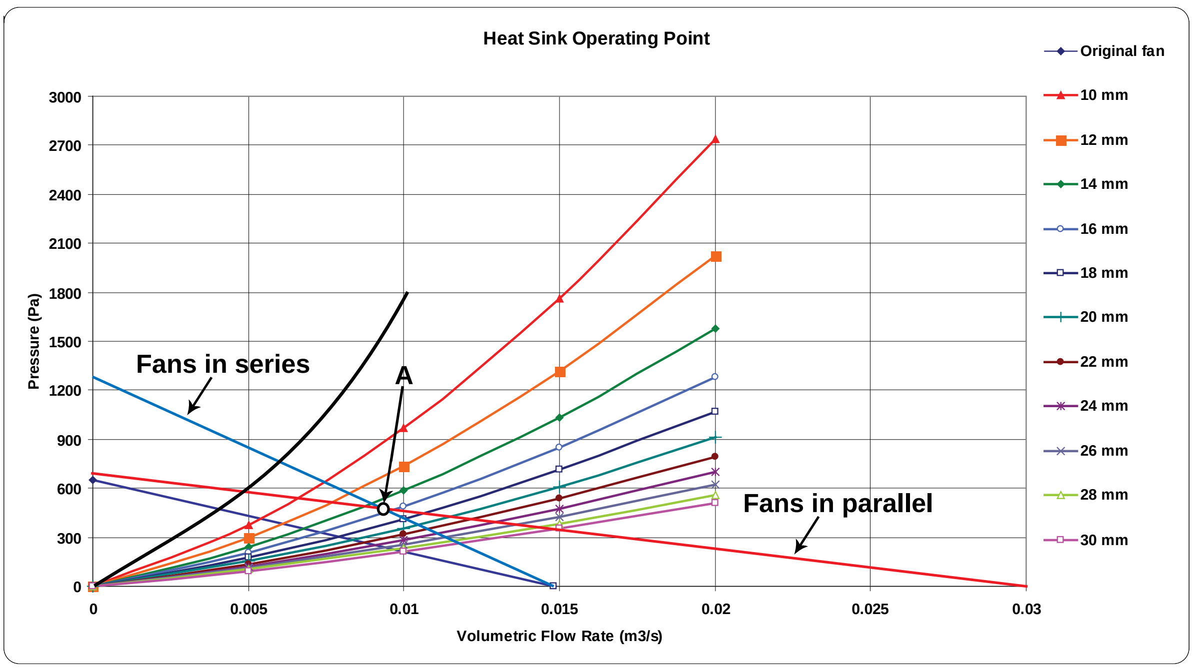


Figure 7. Thermal Resistance of the 80 x 80 mm Heat Sink as a Function of Fin Height.

Figure 8 shows the heat transfer coefficient as a function of fin height. It can be seen that the heat transfer coefficient decreases as height increases. The dip in the heat transfer coefficient at 14 mm of height can be explained by referring to Figure 9. Figure 9 shows that the volumetric flow rate at 14 mm has a dip in volumetric flow rate which causes the dip in the heat transfer coefficient. The dip in the volumetric flow rate is due to the nonlinear nature of the fan curve and heat sink pressure curve operating point. Figure 10 also shows that fin efficiency as a function of fin height constantly decreases. These graphs show that even though the heat transfer coefficient and the efficiency drop, because the overall surface area has increased, the net effect is a decrease in thermal resistance.

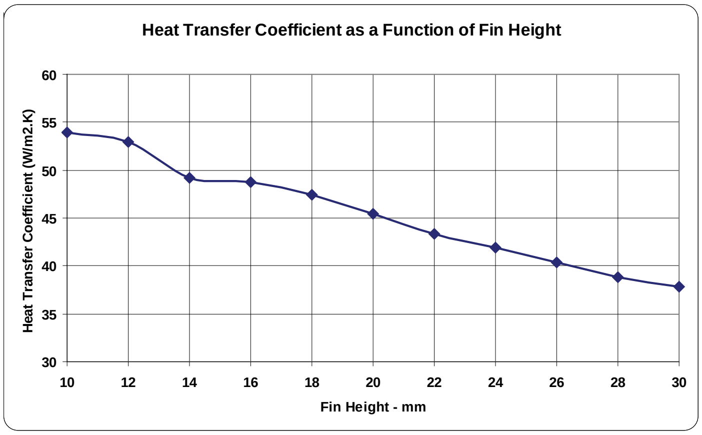


Figure 8. Heat Transfer Coefficient of the 80 x 80 mm Heat Sink as a Function of Fin Height.

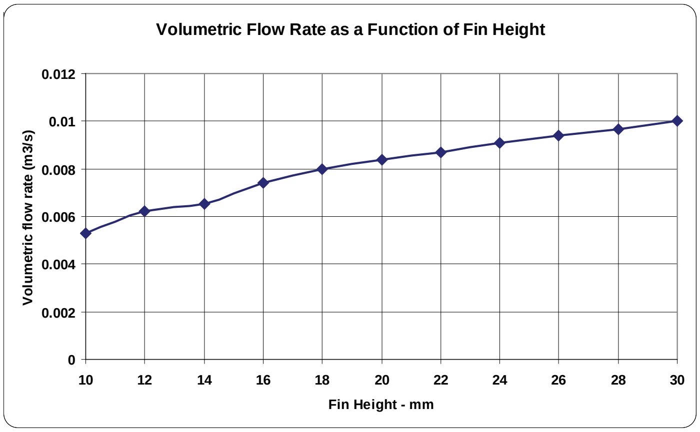


Figure 9. Volumetric Flow Rate of the 80 x 80 mm Heat Sink as a Function of Fin Height.

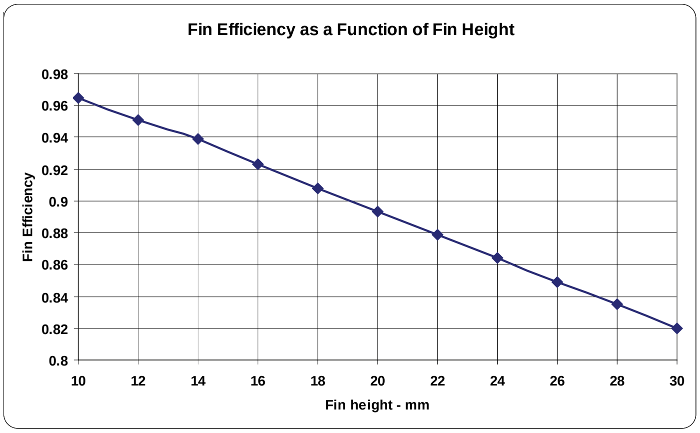


Figure 10. The Fin Efficiency of the 80 x 80 mm Heat Sink as a Function of Fin Height.

Future articles will discuss the optimization of a heat sink by changing both the number of fins and the fin height. The above analysis is a purely theoretical practice. In a real life situation, there might not be the luxury of using a very tall heat sink due to space constraints and, more importantly, because of the manufacturing difficulty in making taller fins. In these circumstances, engineers should look at all the variables and try to optimize based on what is available.

References

1. Azar, K. and Tavassoli, B., How Much Heat Can Be Extracted From a Heat Sink, Electronics Cooling, January 2003.
2. Teerstra, P. and Yovanovich, M., Analytical Forced Convection Modeling of Plate Fin Heat Sinks, Proceedings of 15th IEEE Semi-Therm Symposium, 1999.
3. Culham, J. and Muuzychka, Y., Optimization of Plate Fin Heat Sinks Using Entropy Generation Minimization, IEEE Trans. Components and Packaging Technologies, 2001.
4. Advanced Thermal Solutions, Inc., Qpedia eMagazine, How a Heat Sink's Height Affects Its Thermal Resistance, August 2008.
5. Advanced Thermal Solutions, Inc., Qpedia eMagazine, The Limit of Heat Sink Thermal Resistance for a Ducted Flow, October 2008.


Heat issues have you tangled up?
LET THE EXPERTS AT ATS SHOW YOU HOW TO ENSURE PRODUCT RELIABILITY, SPEED TIME-TO-MARKET AND REDUCE COSTS WITH EXPERT THERMAL MANAGEMENT ANALYSIS AND DESIGN SERVICES.

Heat Sink Testing Methods

and Common Oversights

Introduction

The effective use of an electrical component is limited by its maximum operational junction temperature. To achieve a desired component temperature, excess heat dissipated by the device must be transferred to the environment [1]. The most common method for transferring heat from the component to the environment is to use a heat sink.

To estimate a component's junction temperature, a required value is the heat sink's thermal resistance. The thermal resistance of a heat sink can be determined analytically or experimentally. This article looks at three experimental methods of testing heat sinks.

First, it is necessary to understand the heat transfer path from the component to the local ambient, and then to understand the differences between the practical and experimental application of a heat sink.

Heat Sink Mounted On a Component: Practical Use

In a practical application, the heat transferred to the air from multiple junctions of a component follows a complex 3D heat transfer path. Simplified, the heat transferred from the junction of a component, $\dot{Q}_j$, to the air follows two heat transfer paths, as shown in Figure 1. The first heat transfer path is from the junction to the air via the heat sink $\dot{Q}_{j-a,hs}$. The second path is also from the junction to the air, but via the board $\dot{Q}_{j-a,brd}$. The portion of heat transfer via the heat sink depends on the thermal resistance of the two paths.

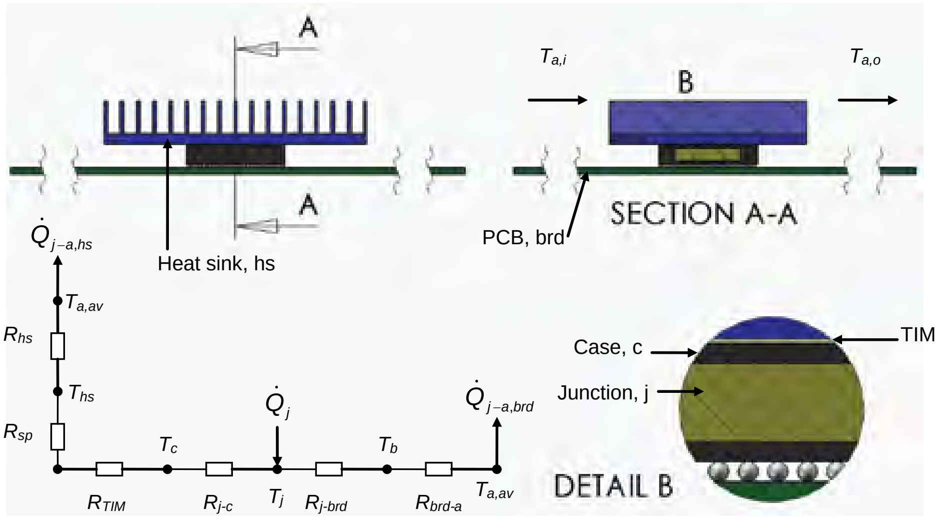


Figure 1. Heat Sink Applied to a Component, Mounted on a Board.

For BGA components without a heat sink, heat transfer to a board is typically 80% of the total heat transfer rate. When a heat sink is mounted to the BGA, the thermal resistance from the case to the air is decreased. Heat transfer to the board will decrease and more heat will be transferred to the air.

Heat Sink Set Up for Testing

A research quality wind tunnel, air temperature and velocity sensor, thermocouples and a power supply are needed to test heat sinks. A resistor is used to dissipate electrical power in the form of heat energy. The resistor is typically attached to the heat sink using thermally conductive double-sided tape. Such tape also attaches the resistor to a board, which is typically a low thermal conductivity printed circuit board or FR4.

As with a heat sink mounted on a component, the heat dissipated in the resistor is transferred to the environment by two paths. However, the thermal resistance from the resistor to the heat sink and to the board is only the interface resistance, R_{TIM}. Heat transfer to the air via the heat sink, $\dot{Q}_{r-a,hs}$ will not equal the energy dissipated in the resistor. If this value is used, there will be an error in determining the thermal resistance of the heat sink because the energy dissipated, $\dot{Q}_r$, is not the heat transfer to the environment via the heat sink.

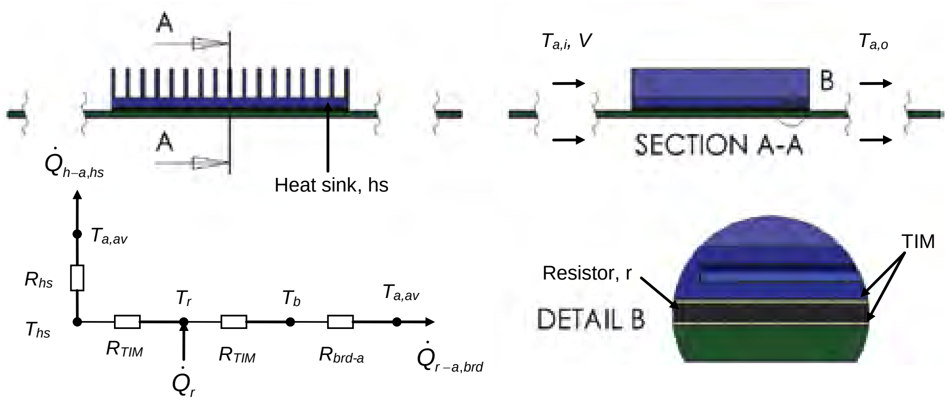


Figure 2. Heat Sink Experimental Set Up.

Thermal resistance from the board to the air increases with decreasing board thickness. Resistance decreases with increasing board thermal conductivity and increased air flow velocity across the board. Though, as previously stated, a low thermal conductivity printed circuit board is used to minimize the loss through the board.

Heat Sink Experimental Set Ups

The first method of heat sink testing is set up in an unducted environment. This is similar to the flow experienced in typical applications. The airflow through the heat sink is affected by its fin density. The higher the fin density, the more airflow bypasses the heat sink. This provides realistic data for the thermal performance of the heat sink. The test is easy to set up, but requires a higher quality testing facility. One

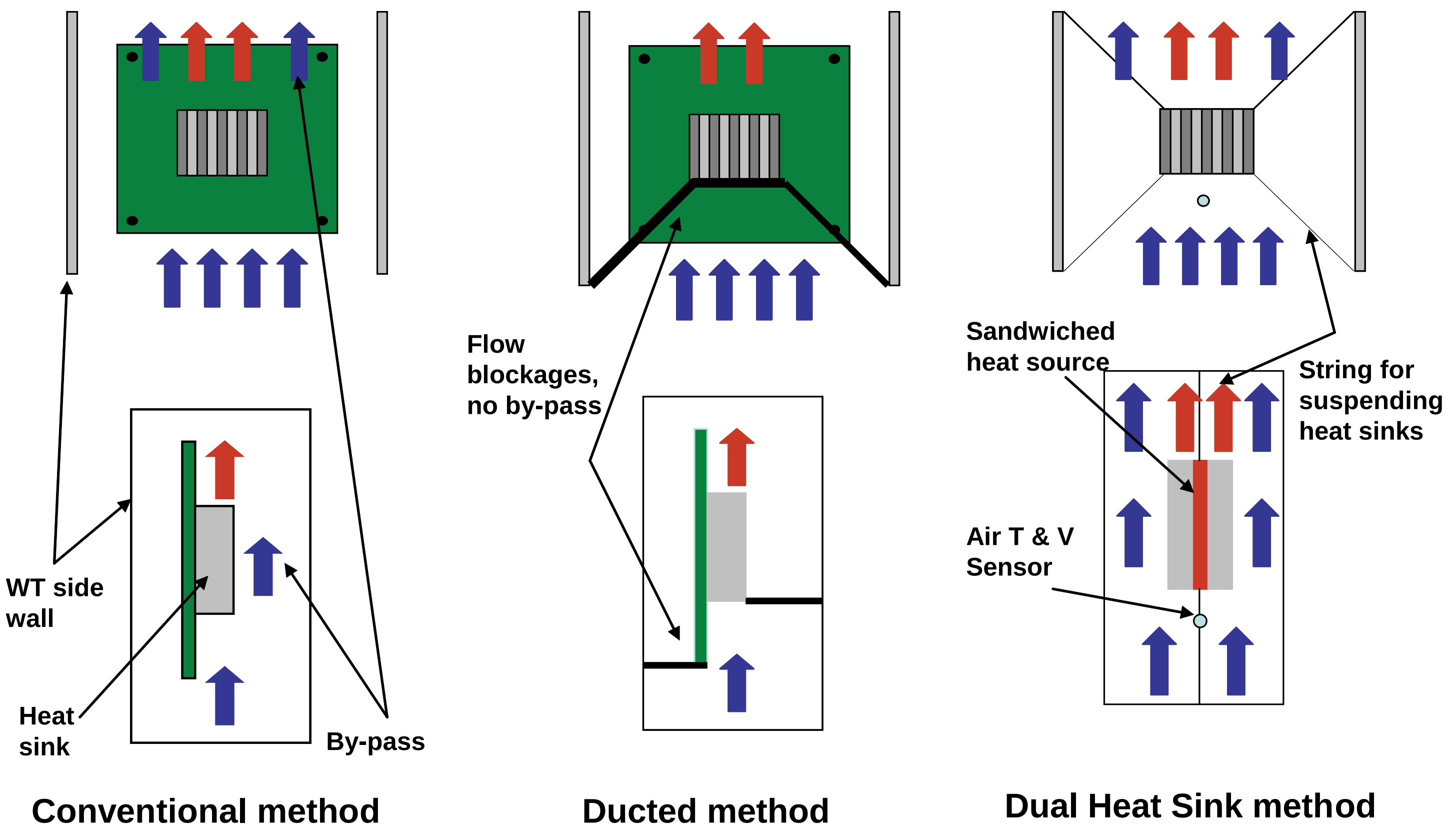


Figure 3. Heat Sink Experimental Set Ups: Unducted (a), Ducted (b) and Dual Heat Sink Testing Methods [3].

prominent issue is that the heat loss to the board must be taken into account.

The second method of heat sink testing is set up in a duct. This forces all of the airflow to go through the heat sink. There is no air flow around the heat sink or bypass airflow. It is moderately easy to set up. Vendor supplied thermal resistance data is commonly provided for ducted test results. However, the results are optimistic and can give misleading data when heat sinks are used in an unducted application.

The third method is dual heat sink testing, which uses two identical heat sinks with a heater sandwiched between them. The assembly is suspended on the centerline of a research quality wind tunnel. Dual heat sink testing is a good approach because there are no heat transfer losses to the air, e.g. via a board. But this method is rarely used in industry because it is time consuming to set up and because the approach velocity is difficult to measure without using a quality testing facility.

Example of a Heat Sink Testing Results

To show the differences in thermal resistances, as determined by each testing method, we can compare the resistances of a maxiFLOW™ and a straight fin heat sink. The maxiFLOW heat sink has a base size of 42.5 x 42.5 mm, and is 17.5 mm high. However, the straight fin heat sink has a base size of 80 x 76 mm and is 20 mm high. Due to these size differences, the thermal resistance of the smaller maxiFLOW sink will be higher than that of the straight fin heat sink. The straight fin sink is 284% bigger in volume than the maxiFLOW heat sink.

As shown in Table 1, the maxiFLOW heat sink has a thermal resistance of 1.5 K/W when ducted, and 1.9 K/W when unducted at 1 m/s,. This results in a 21% difference between the testing methods. The dense straight fin heat sink was simulated using CFD. It has a ducted thermal resistance of 0.38 K/

Table 1. Ducted and Unducted Thermal Resistance of an ATS-52425P-C2-R0 at ~1 m/s (200 LFM) (42.5 x 42.5 x 17.5 mm) [2].

Test Environment	Thermal resistance [K/W]	Difference between thermal resistances [%]
Ducted	1.5	-21%
Unducted	1.9	Datum

Table 2. Ducted, Unducted and Dual Thermal Resistance of a Straight Fin Heat Sink at 1 m/s (~200 LFM) (80 x 76 x 20 mm).

Testing Method	Base Temperature [ºC]	Thermal Resistance [K/W]	Difference Between Thermal Resistances [%]	Pressure Drop [Pa]
Ducted	23.8	0.38	-71%	40
Unducted	33.1	1.31	Datum	2.0
Dual	34.7	1.47	12%	2.4

W, and resistance of 1.31 K/W when unducted as shown in Table 2. This results in a difference of 71%. The large difference in thermal resistance between testing methods is due to the dense fins. Airflow goes around the heat sink in an unducted test, as shown by the particle tracks in Figure 5. All of the particle tracks go through the heat sink in the ducted simulation, as shown in Figure 4.

Simulated as a dual heat sink, the thermal resistance differs by 12%. This is due to the heat loss to the environment via the FR4 board.

Summary

Heat sink manufacturers often report ducted test data, but most practical applications involve an unducted heat sink. Unducted thermal resistance data can be 20% higher or more than ducted data. It is essential that the design engineer makes sure what test data to use. Failure to do so can have serious implications for the reliability of the hot components. Table 3 provides a summary of the heat sink testing methods.

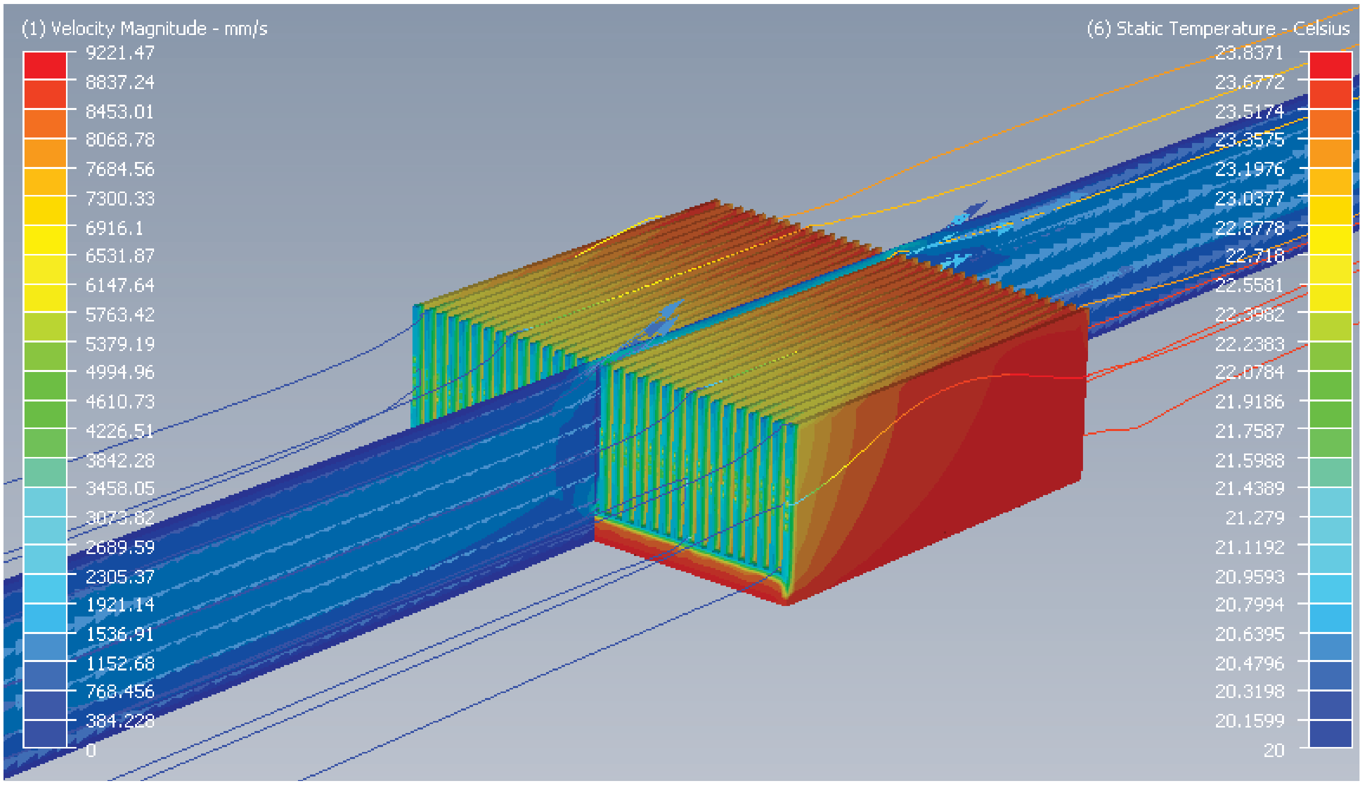


Figure 4. CFD Image of a Straight Fin Heat Sink in a Ducted Environment, Dissipating 10 W at an Inlet Air Flow Velocity of 1 m/s (~200 LFM).

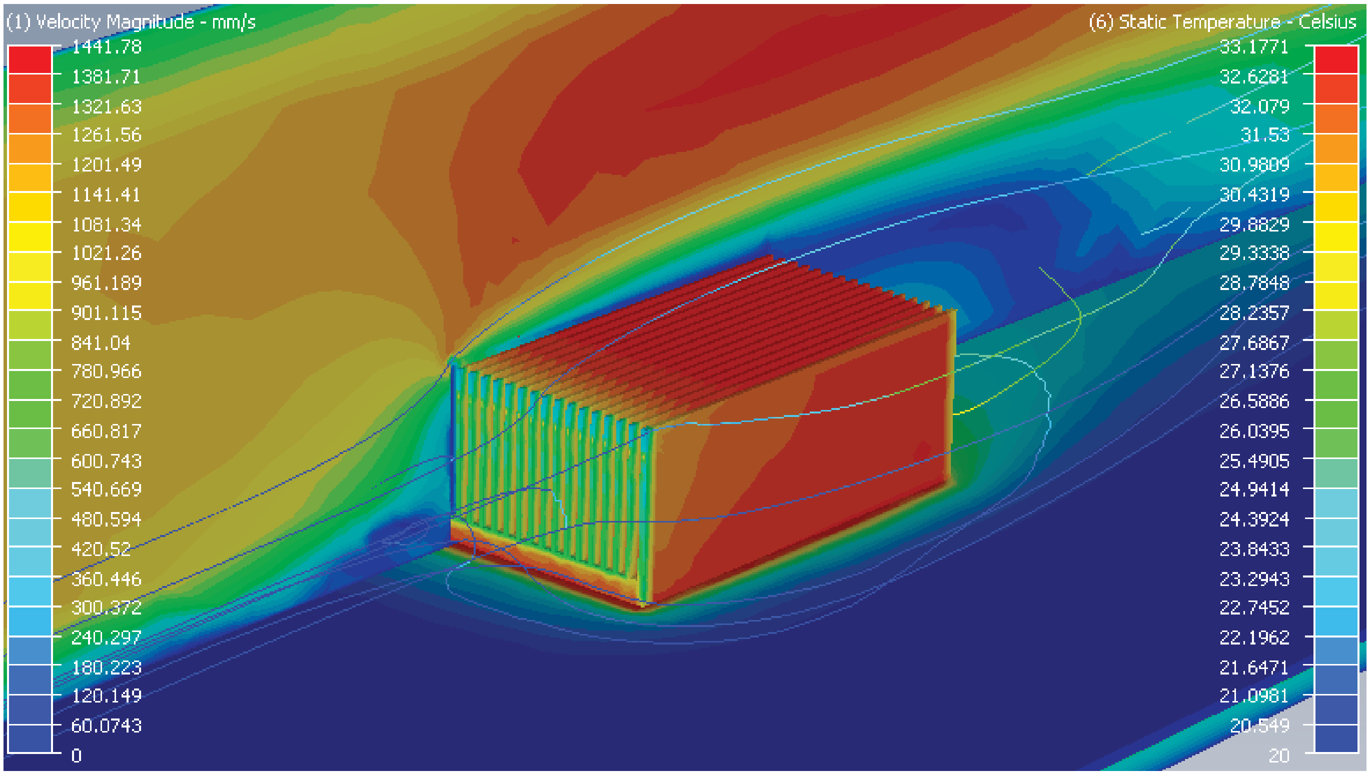


Figure 5. CFD Image of a Straight Fin Heat Sink in an Unducted Environment, Dissipating 10 W at an Inlet Air Flow Velocity of 1 m/s (~200 LFM).

Table 3. Summary of Heat Sink Testing Methods

Method	Description	Pros	Cons
Unducted	Place heat sink on a heat source on a board and suspend assembly in the middle of a wind tunnel.	A better method for thermal characterization. Relatively easy to setup. Provides realistic data that corresponds to application.	Must accurately account for the heat coming through the heat sink. Requires a quality testing facility.
Ducted	Force the entire flow through the heat sink and provide no room for bypass flow.	Most commonly practiced by heat sink vendors because it shows superior data. Moderately easy to setup.	It provides far too optimistic thermal resistance that is misleading for unducted applications.
Dual Heat Sink	Use two identical heat sinks with a heater sandwiched in between; suspend the assembly in the wind tunnel.	No heat losses due to a board. Rarely practiced in the industry.	Time consuming to set up. Requires care for measuring the approach air velocity and temperature. Requires a quality testing facility.

References

1. Sergent, J. and Krum, A., Thermal Management Handbook for Electronic Assemblies, First Edition, McGraw-Hill, 1998.
2. Advanced Thermal Solutions, Inc., Data Sheet for maxiFLOW ATS-52425P-C2-R0
3. Advanced Thermal Solutions, Inc. Heat Sink Design and Characterization, Tutorial.

Conduction Heat Transfer

and How it is Calculated

Introduction

Conduction heat transfer is the spontaneous transfer of heat energy through a material due to temperature gradient. This process continues as long as a temperature gradient exists in the material. The governing equation is known as Fourier's law of heat conduction for one dimension [1].

$$q = -kA\left(\frac{\partial T}{\partial x}\right) \tag{1}$$

Where,

q = rate of heat transfer (W)
k = conduction heat transfer coefficient (W/m/°C)
$\frac{\partial T}{\partial x}$ = temperature gradient in the direction of the heat flow

This equation shows that the rate of heat transfer per unit area is directly proportional to the temperature gradient between the points of conduction, and k (the conductive heat transfer coefficient) is the proportionality constant.

To illustrate the role of conduction heat transfer, we will consider a typical heat transfer analysis problem, involving convection and radiation, and derive the necessary differential equations to predict the heat transfer behavior. Finally, we will solve the differential equation for a baseline case.

Discussion

A heat transfer analysis was performed on the cylindrical pin fin shown in Figure 1 below.

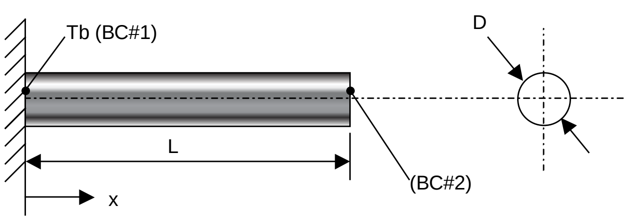


Figure 1. Description of Pin for Heat Transfer Analysis.

For this problem, the boundary conditions are assumed to be known at the base and tip of the pin. To develop a differential equation describing heat conduction through the pin and subsequent heat removal due to convection and radiation, an energy balance is performed on a differential element of the pin. This is shown in Figure 2.

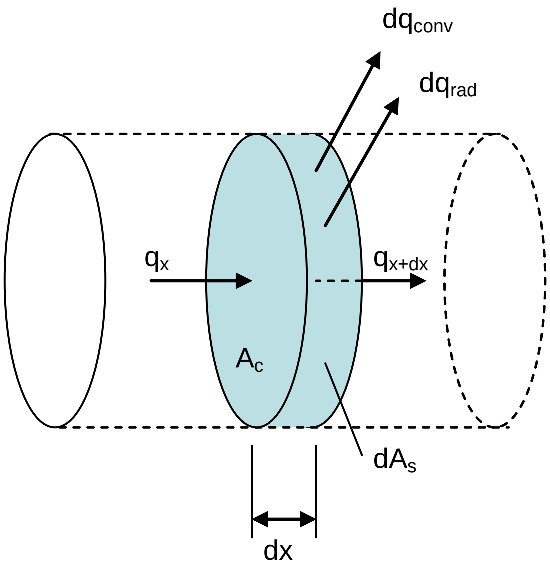


Figure 2. Differential Cylindrical Element.

The following equation results:

$$q_x = q_{x+dx} + dq_{conv} + dq_{rad} \tag{2}$$

Here q_x is the energy into the left face of the differential element and q_{x+dx} is the energy out of the right face of the element. The terms dq_{conv} and dq_{rad} represent the energy lost by convection and radiation, respectively, for the differential slice. For this problem the energy generation terms have been neglected. The term q_{x+dx} can now be written in terms of the Taylor series expansion [2].

$$q_{x+dx} = q_x + \frac{dq_x}{dx}dx \tag{3}$$

Substituting (3) into (2) results in a new equation (4).

$$-\frac{dq_x}{dx}dx = dq_{conv} + dq_{rad} \quad (4)$$

This equation basically says that the difference between the conduction heat transfer into and out of the differential element is equal to the sum of the convection and radiation heat transfer from the surface of the element to the environment.

Substituting the dimensional equations for conduction, convection and radiation in (4), and noting that the surface area on the perimeter of the pin on a differential basis can be written as $dA_s = \pi D dx$; and finally dividing through by dx the following equation emerges.

$$\frac{d}{dx}\left(kA_c\frac{dT}{dx}\right) = h_c\pi D(T - T_\infty) + h_r\pi D(T - T_{sur}) \quad (5)$$

Where T_{sur} is the temperature of the radiating surface. Because both the thermal conductivity k and the Area of conduction A_c remain constant for this example, (5) reduces to (6) below.

$$\frac{d^2T}{dx^2} = \frac{h_c\pi D}{kA_c}(T - T_\infty) + \frac{h_r\pi D}{kA_c}(T - T_{sur}) \quad (6)$$

This is the governing differential equation. In order to solve this equation and gain some insight into what is going on, we need to define an expression for the convective heat transfer coefficient. If we assume natural convection, we can use the following equation (7) as a typical correlation [2].

$$h_c = 2.890\left[0.6 + 0.624(T + T_\infty)^{1/6}\right]^2 \quad (7)$$

Defining a radiation heat transfer coefficient as follows:

$$h_r = \varepsilon\sigma(T + T_{sur})(T^2 + T_{sur}^2) \quad (8)$$

And with the BC (boundary conditions) shown in (9) and (10) below:

BC - 1, at x = 0

$$T(0) = T_b \quad (9)$$

BC - 2, at x = L

$$-kA_c\left.\frac{dT}{dx}\right|_{x=L} = h_cA_c(T(L) - T_\infty) + h_rA_c(T(L) - T_{sur}) \quad (10)$$

The governing differential equation can now be solved for the temperature distribution T along the length of the pin. With T known, the total heat transfer q_{tot}, and the contributions from convection and radiation (q_{conv} and q_{rad}) can be calculated using (11), (12), and (13) below.

$$q_{tot} = -kA_c\left.\frac{dT}{dx}\right|_{x=0} \quad (11)$$

$$q_{conv} = \int dq_{conv} = \int h_c\pi D(T - T_\infty) + h_c\pi D(T - T_\infty)\Big|_{x=L} \quad (12)$$

$$q_{rad} = \int dq_{rad} = \int h_r\pi D(T - T_{sur})dx + h_rA_c(T - T_{sur})\Big|_{x=L} \quad (13)$$

Table 1. Baseline Values for Use in Calculating Heat Transfer for the Pin Style Fin.

Description	Variable	Value	Units
Pin Base Temperature	T_b	100	ºC
Surrounding Temperature	T_∞	25	ºC
Length of Pin	L	10	cm
Diameter of Pin	D	1	cm
Thermal Conductivity	k	14	W/mK
Emissivity	ε	0.2	-
Stefan-Boltzmann Constant	σ	5.67e-8	W/m^2K^4

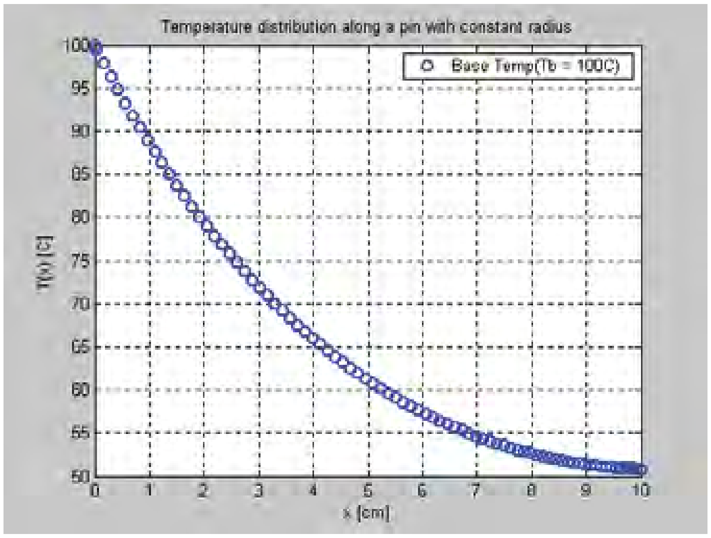


Figure 3. Baseline Temperature Profile for Length of Pin.

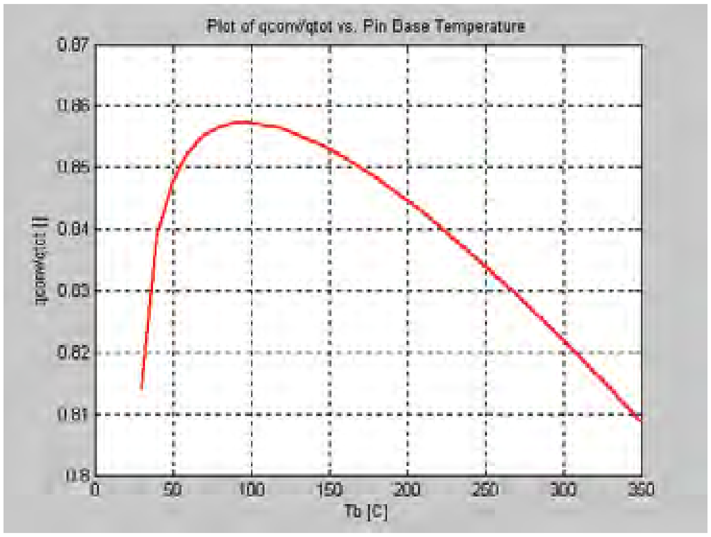


Figure 4. Plot of Convection Heat Transfer with Respect to Total Heat Transfer.

Defining a baseline case for numerical analysis (Table 1), and solving using the Finite Difference method, we get the following temperature distribution for the pin (Figure 3).

It can be seen that the temperature decreases along the length of the pin. This is expected because there are heat transfer losses from convection and radiation as heat conducts down the pin. The temperature decrease is exponential as predicted by Newton's Law of Cooling.

The ratio of the heat loss by convection and radiation with respect to the total heat transfer is shown in Figures 4 and 5 for a base temperature range of 30°C to 350°C. The total heat transfer is equal to the conductive heat transfer at x = 0 (the heat entry point) of the pin. Note that Equation 11 is the Fourier Conduction equation.

These plots show us that approximately 80% of the heat transfer from the pin is due to convection for the baseline case, with the remaining 20% from radiation. When the base temperature of the pin is changed, the temperature distribution, and particularly the temperature gradient at X = 0, will change, resulting in more or less heat conduction into the pin as predicted by Fourier's Law (larger or smaller q_{tot}). The effect of different pin base temperatures shows that there is a point of inflection at approximately 100°C beyond which further increases in temperature will result in an ever greater radiation heat transfer, until this mode becomes dominant.

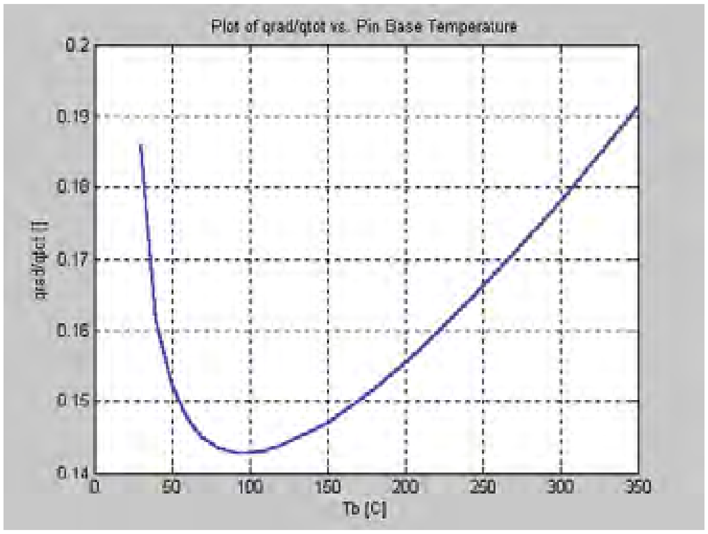


Figure 5. Plot of Radiation Heat Transfer with Respect to Total Heat Transfer.

Conclusion

In this article, we attempted to gain some insight into the role of heat conduction as one of the three major modes of heat transfer, which also include, convection and radiation. We derived the basic differential equations that govern the heat transfer in a pin in a natural convection environment, and we showed how conduction, radiation and convection are related. While this case was for a one-dimensional steady-state condition, it is important to note that the fundamental conduction equation (Fourier's Law) can also be generalized to handle multi-dimensional, transient heat conduction and heat generation.

References

1. Holman, J., Heat Transfer, McGraw-Hill College, Ninth Edition, 2002.
2. White, J., University of Massachusetts Lowell, Math Methods Lecture Notes, Fall 2003.

Qpedia

Getting your company's message out to over 17,000 engineers and industry professionals has never been easier.

Advertise in Qpedia Today!

Qpedia was launched in 2007 as a technology eMagazine focused on the thermal management of electronics. It is designed as a resource to help the engineering community solve the most challenging thermal problems.

The newsletter is published monthly and distributed at no charge to over 17,000 engineers worldwide. Qpedia is also available online or for download at www.qats.com/qpedia. Qpedia's editorial team includes ATS' President & CEO Kaveh Azar Ph.D., and Bahman Tavassoli Ph.D., the company's chief technologist. Both Azar and Tavassoli are internationally recognized experts in the thermal management of electronics.

For more information on how you can generate awareness about your company or products, contace Ray Santos at 782.769.2800.

ATS ADVANCED THERMAL SOLUTIONS, INC.
Innovations in Thermal Management®

www.qats.com | 781.769.2800 | 89-27 Access Road Norwood, MA 02062 USA